

Winery CALPELLA N11M-GE Schematics

Mobile Arrandale

Intel Ixex Peak-M

2010-01-18

www.aitech1.ru
REV : X-build

DY : Nopop Component

UMA : Pop when schematic is UMA

DIS : Pop when schematic is DIS

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
Custom

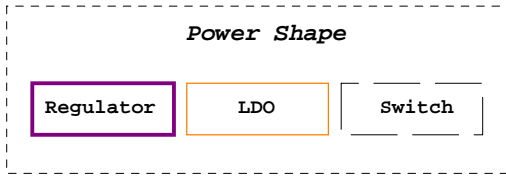
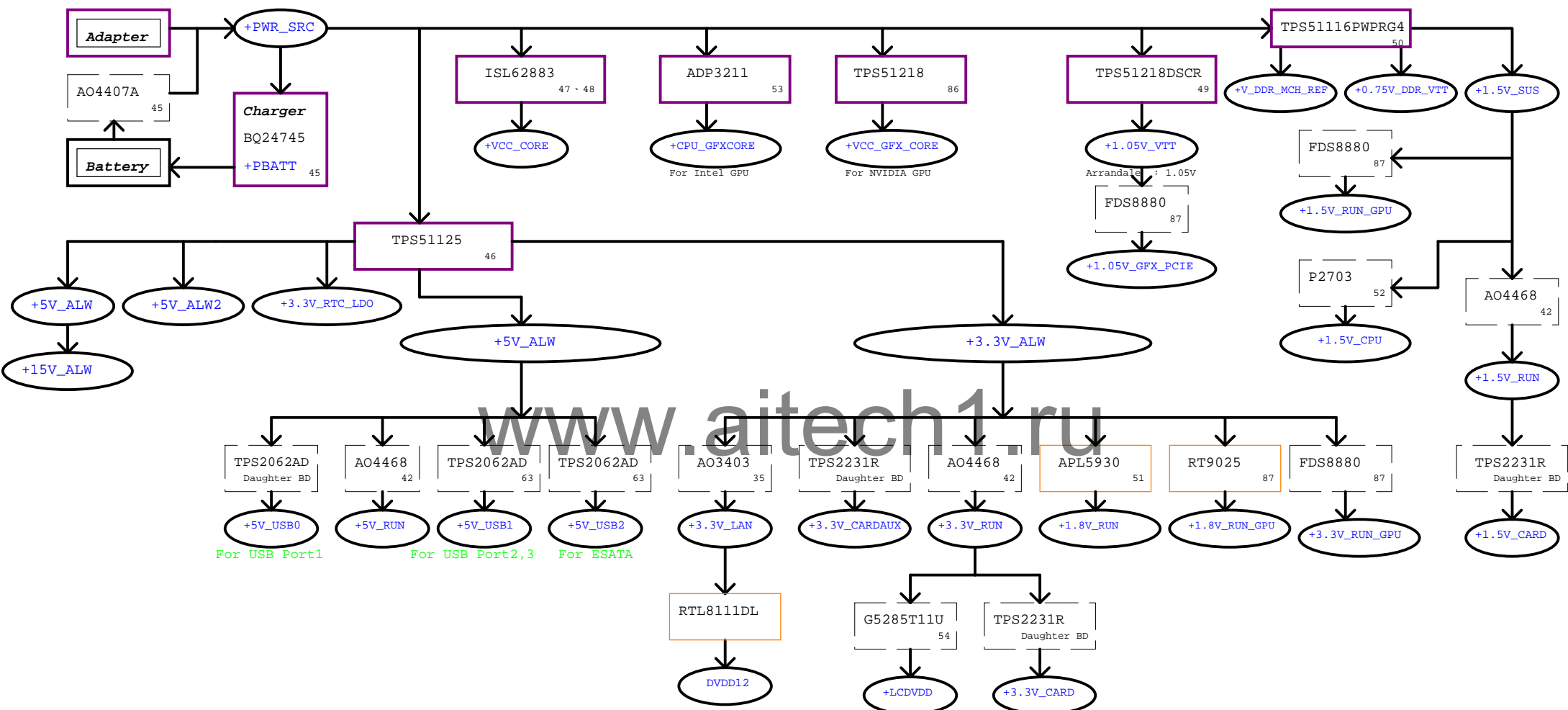
Document Number

Vostro Calpella

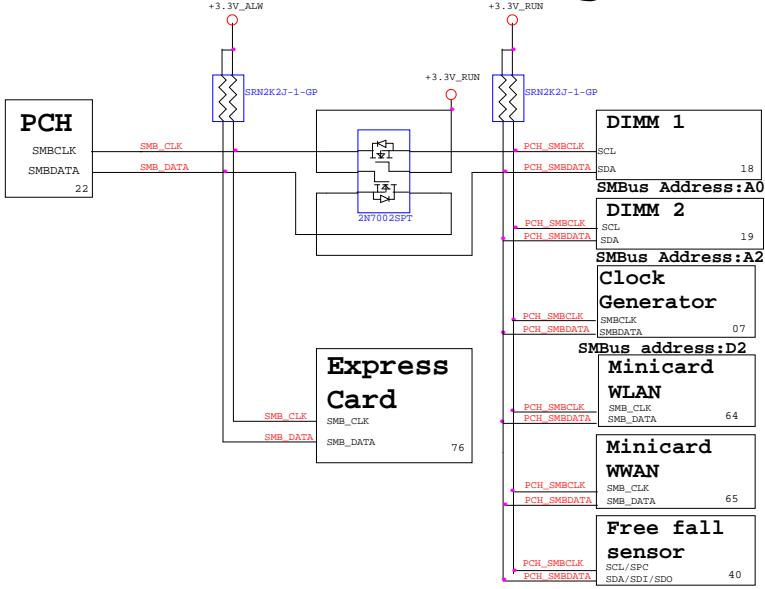
Rev
X01

Date: Monday, January 18, 2010

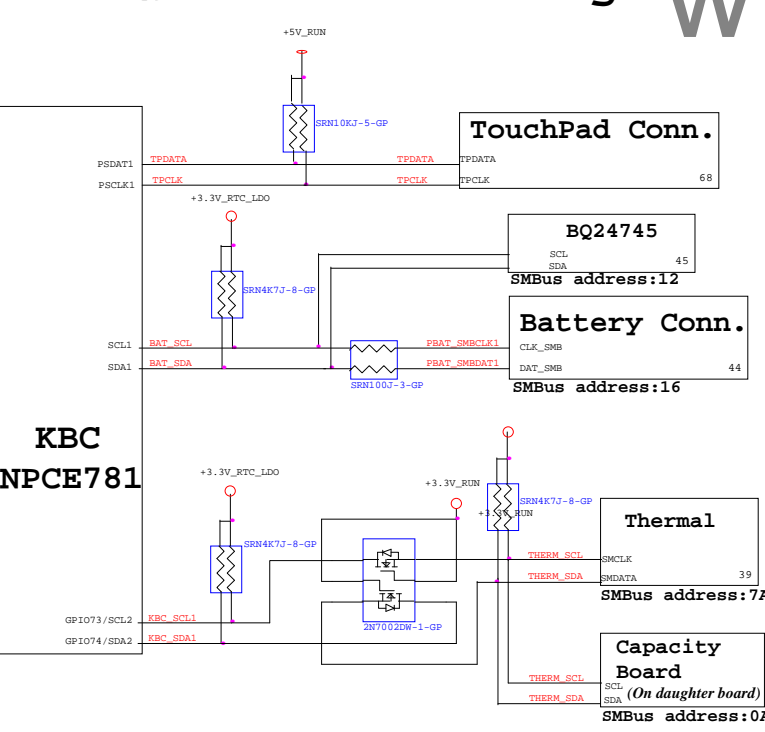
Sheet 1 of 91



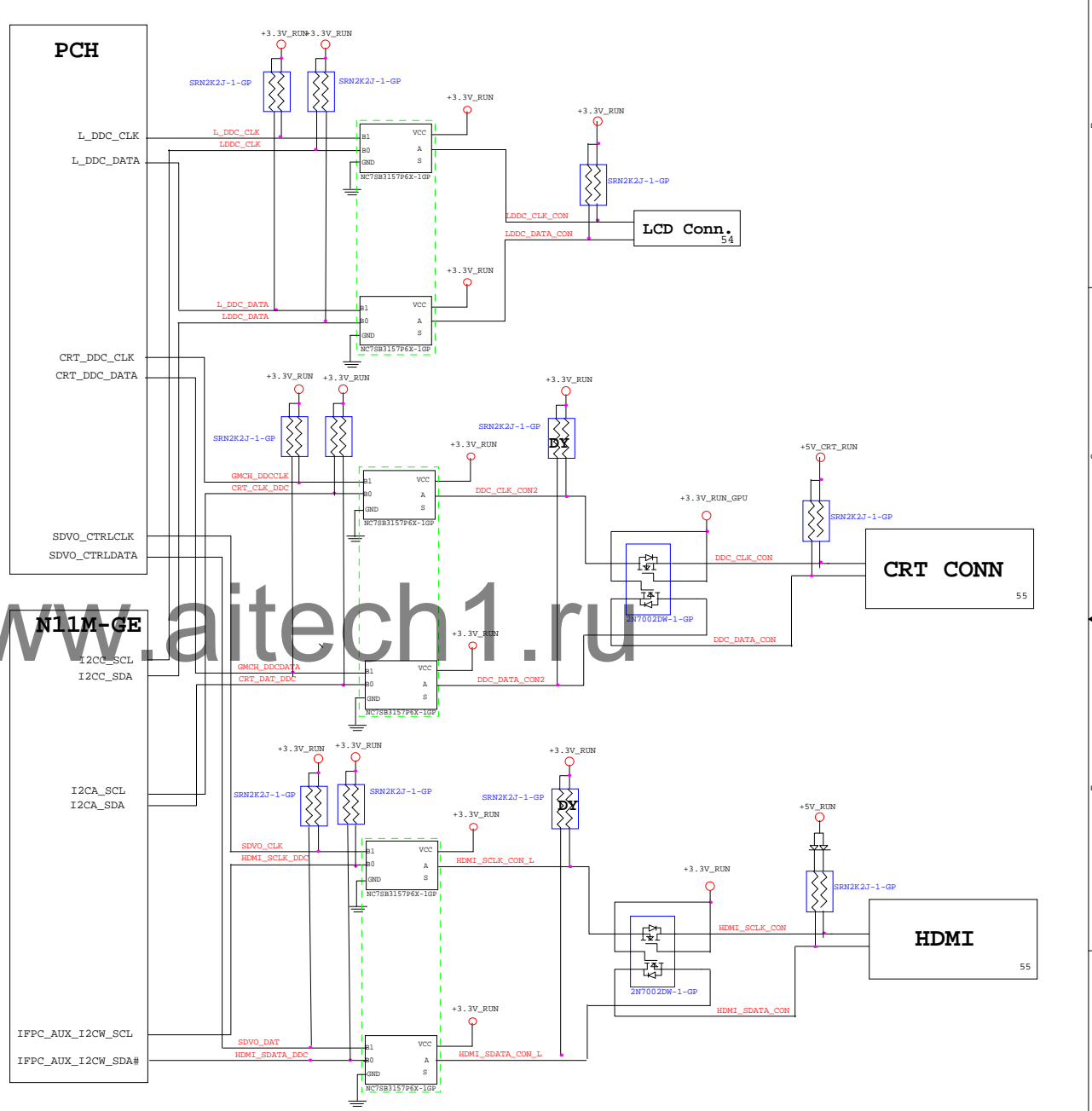
PCH SMBus Block Diagram



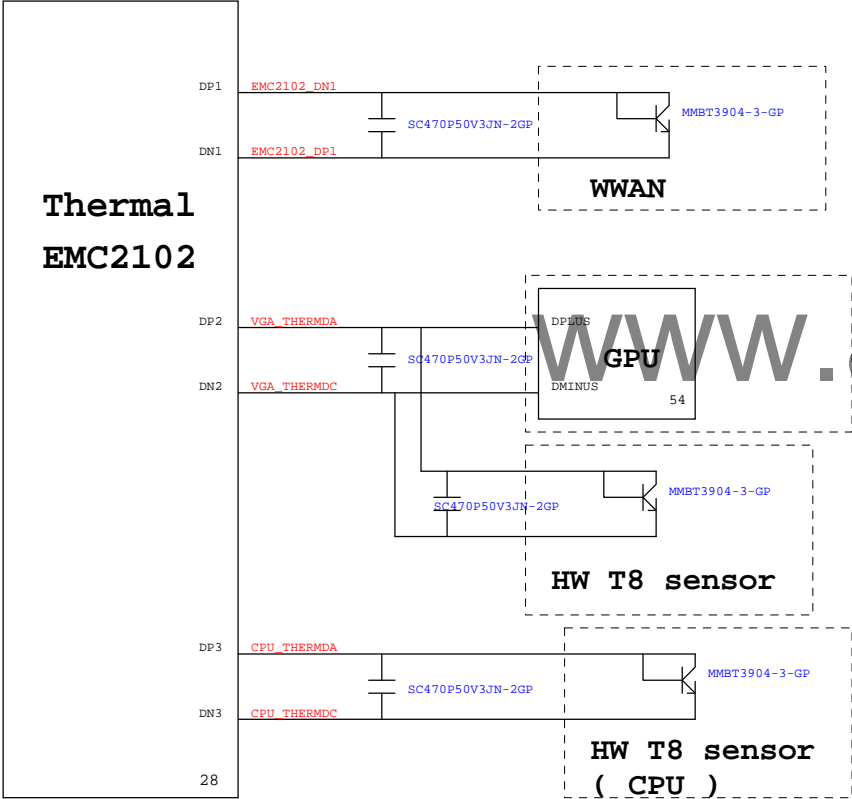
KBC SMBus Block Diagram



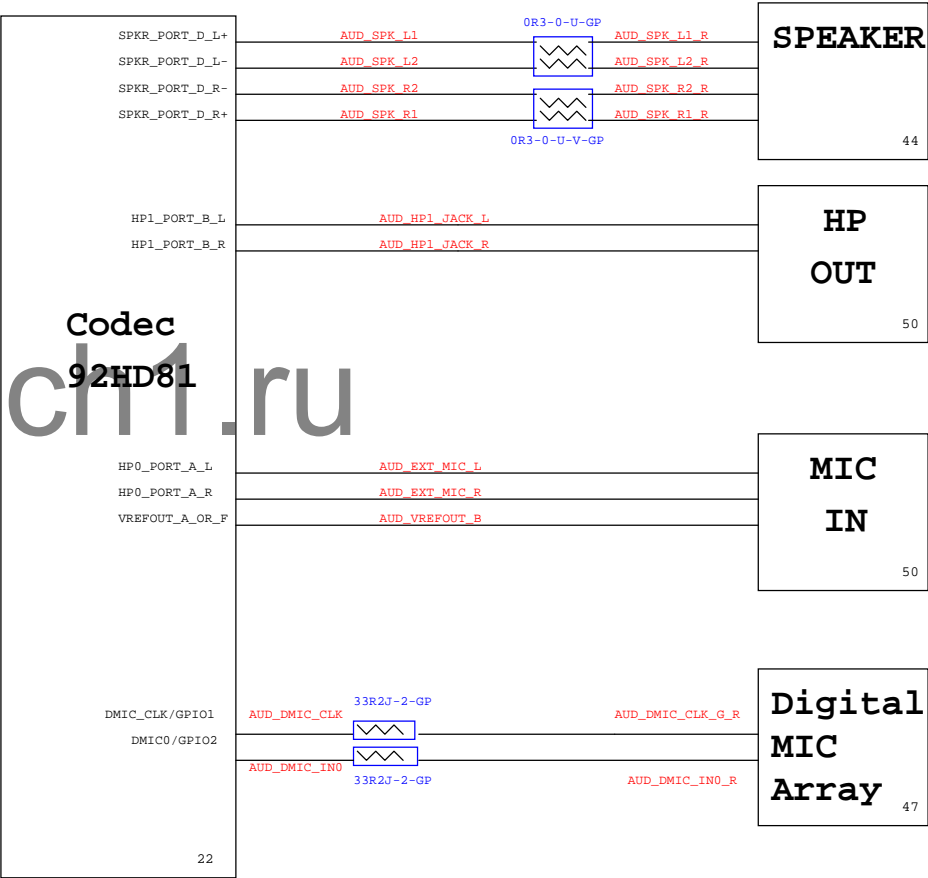
Switchable Graphic SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



PCH Strapping

Calpella Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap ModeNote: Connect to ground with 4.7-kΩ weak pull-down resistor. CRB uses a 1 k do not stuff resistor.
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#/GPIO51	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	Default - Internal pull-up. Low (0)= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIE Routing

LANE1	Card reader
LANE2	MiniCard WLAN
LANE3	LAN
LANE4	MiniCard WWAN
LANE5	New Card

Processor Strapping

Calpella Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

www.aitech1.ru

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Table of Content

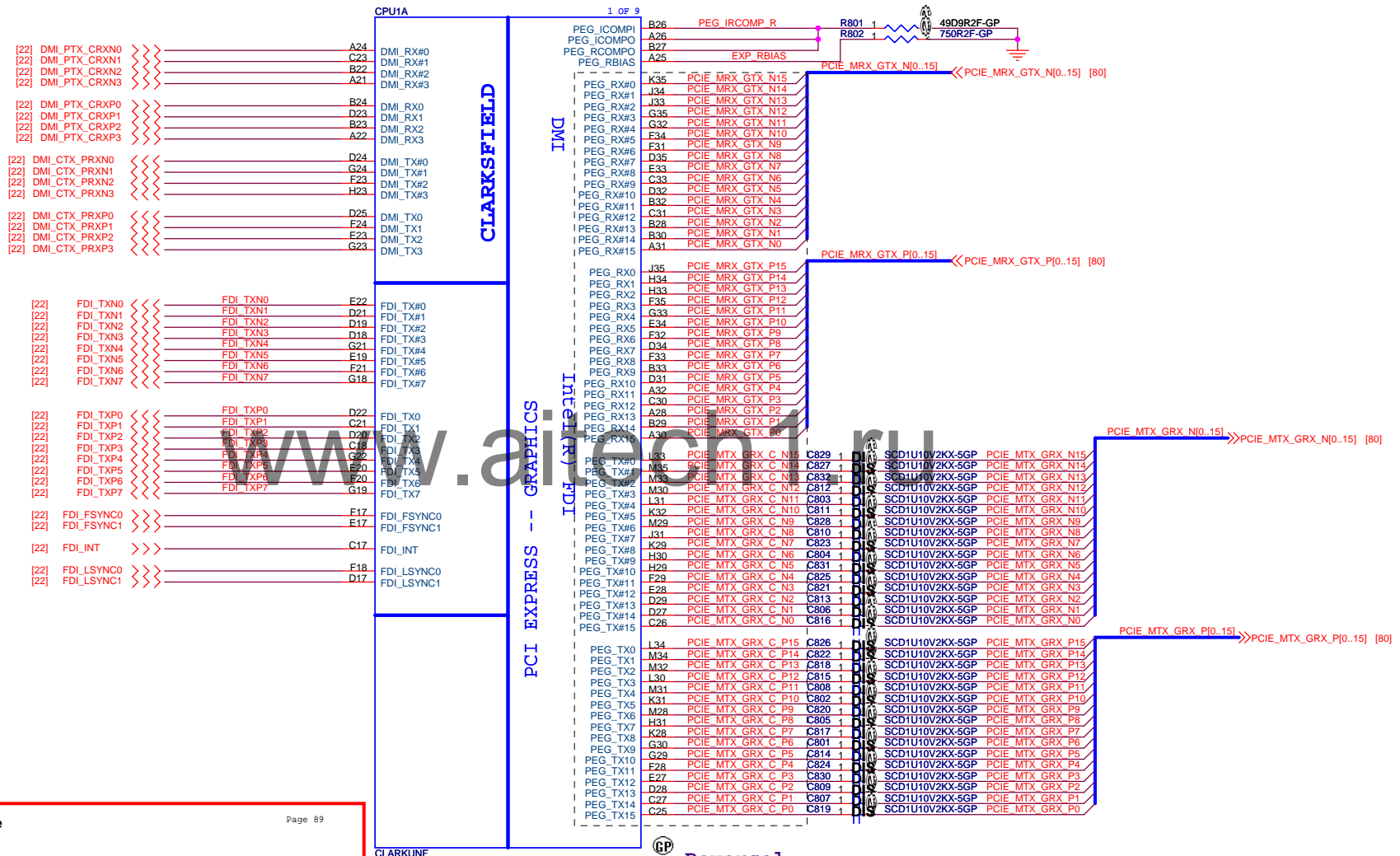
SizeCustom

Document NumberVostro Calpella

RevX01

Date: Monday, January 18, 2010

Sheet6 of91



Calpella Platform Design Guide

Revision 1.6

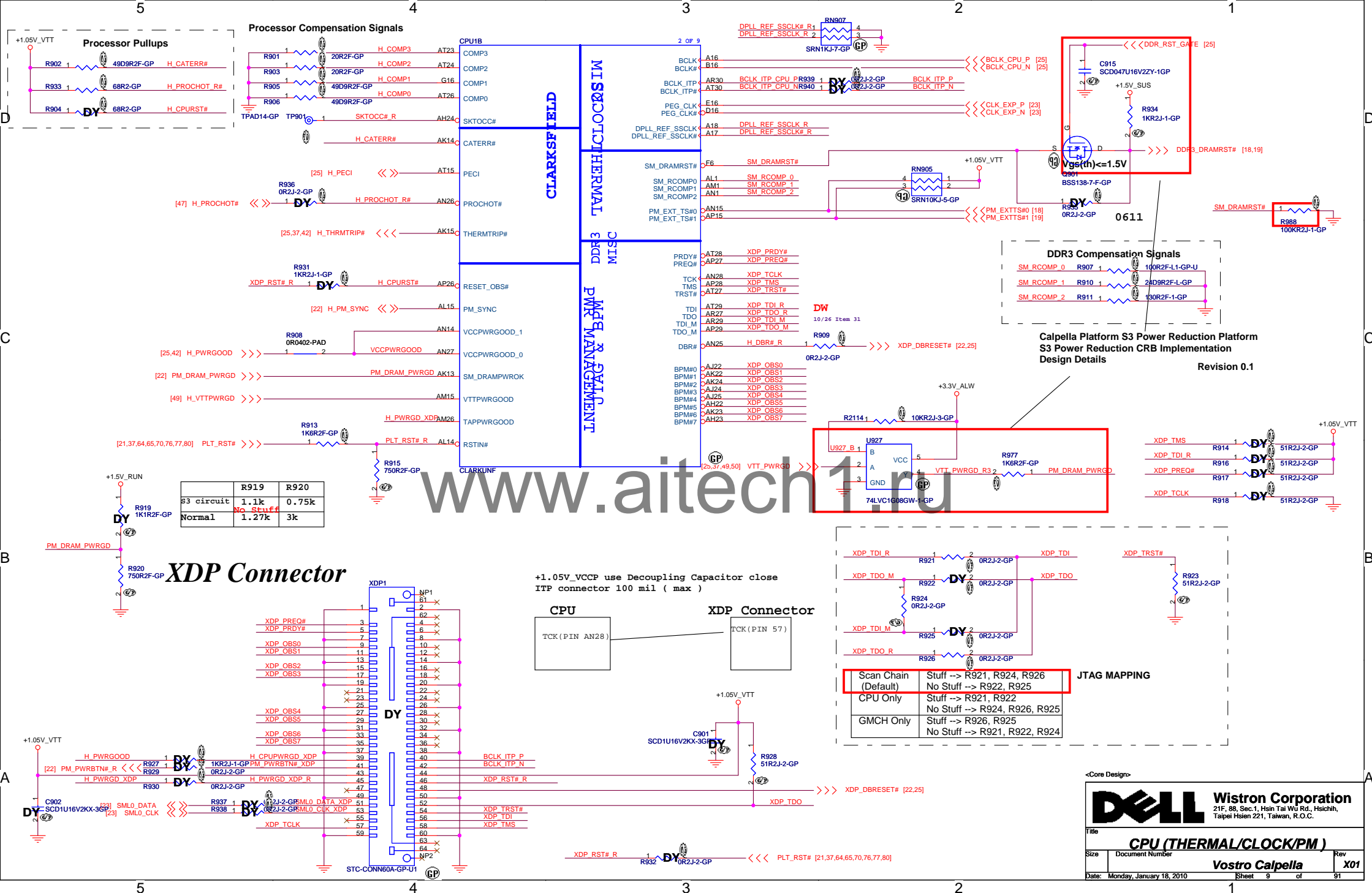
Page 89

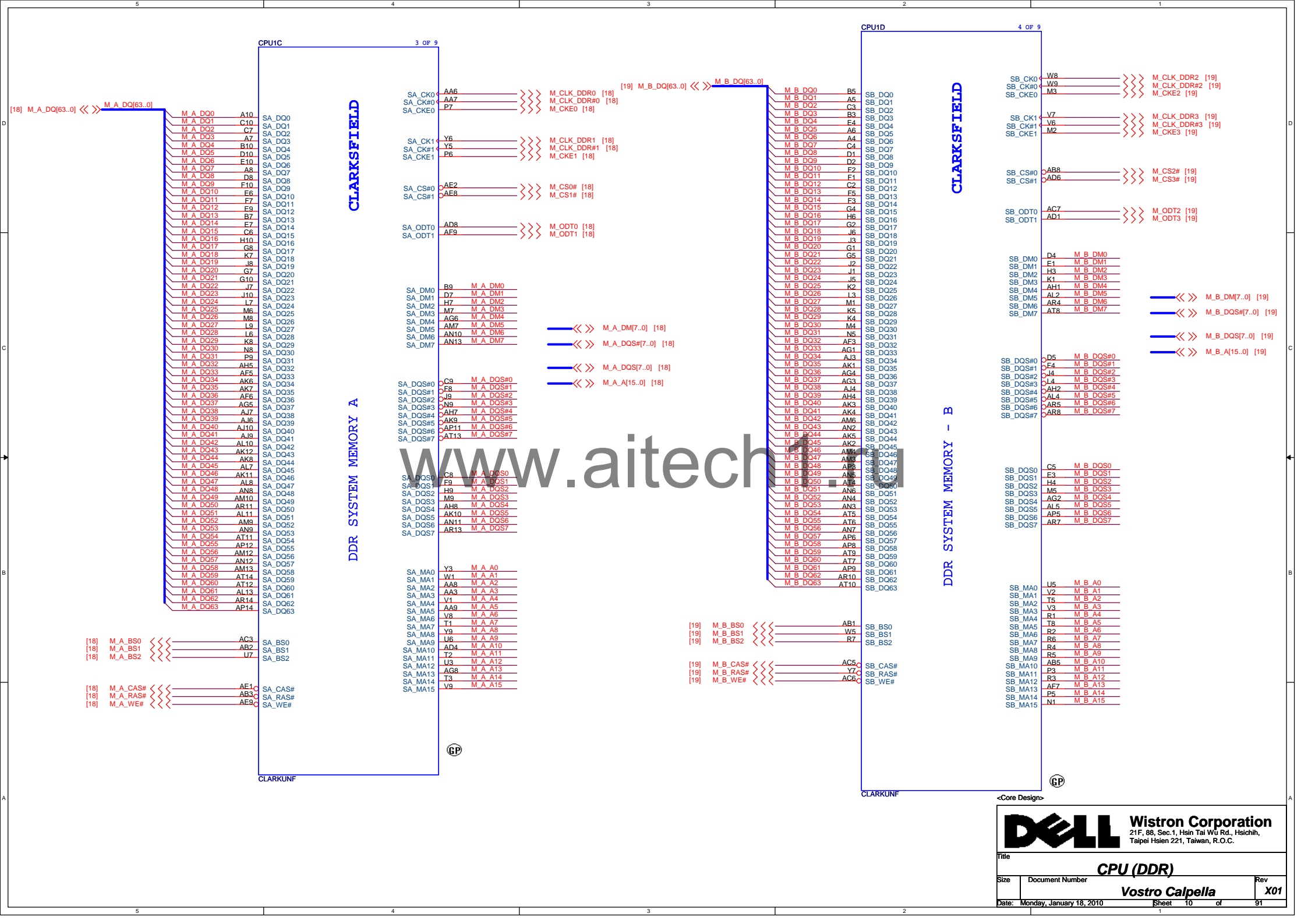
2.4 Arrandale Graphics Disable Guideline

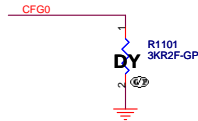
It applies to Arrandale and Clarksfield discrete graphic designs.

FDI_TX[7:0] and FDI_TX# [7:0] can be left floating on the Arrandale. The GFX_IMON, FDI_FSYN0, FDI_FSYN1, FDI_LSYN0, FDI_LSYN1, and FDI_INT signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).

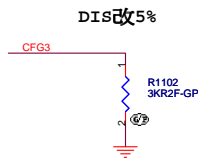
<Core Design>



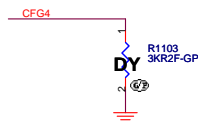




PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled



CFG3 - PCI-Express Static Lane Reversal	
CFG3	1:Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

Calpella Platform Design Guide Revision 1.6

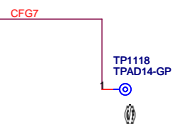
4.8.3.1 LVDS Switching

Switchable GFX, just like integrated GFX only, to enable LVDS it is required that the OEM set the LDVS (L_DDC_DATA) strap to present (pulled up) and the eDP strap (CFG[4]) to disabled (not pulled down).

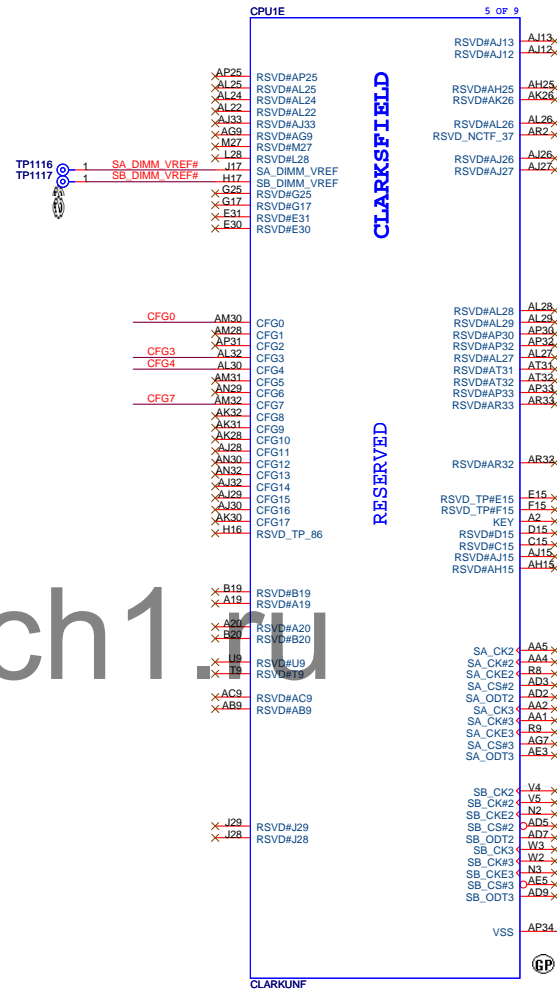
4.8.3.2 eDP Switching

eDP for Switchable GFX can only be driven out of Port D of PCH. To configure Port D for embedded DP it is required to set the DDPD_CTRLDATA strap high to 3.3V Core rail through 2.2 kΩ ±5% resistor, LVDS (L_DDC_DATA) strap as no connect and the eDP strap CFG[4] as no connect.

Page 482,486



CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.

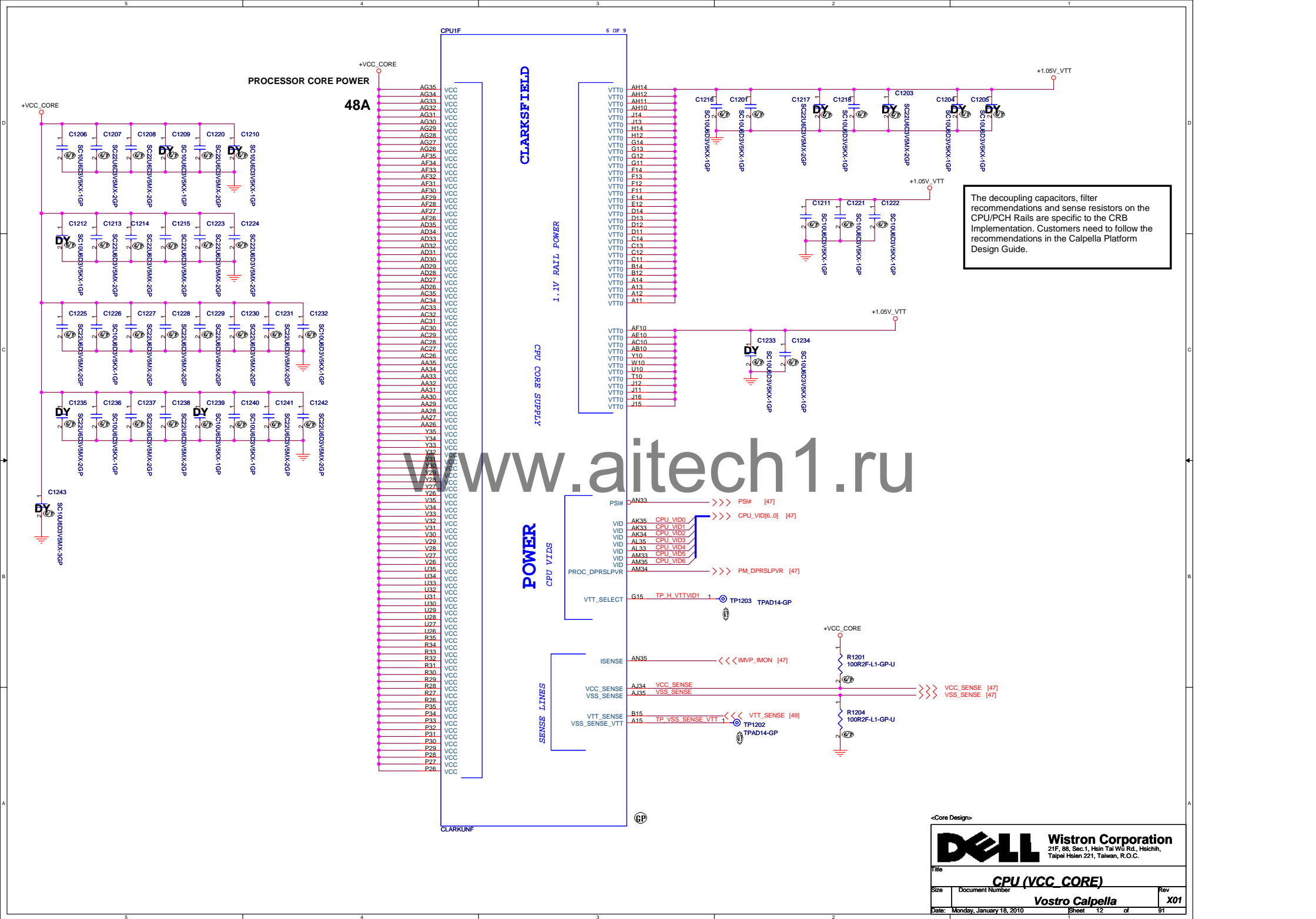


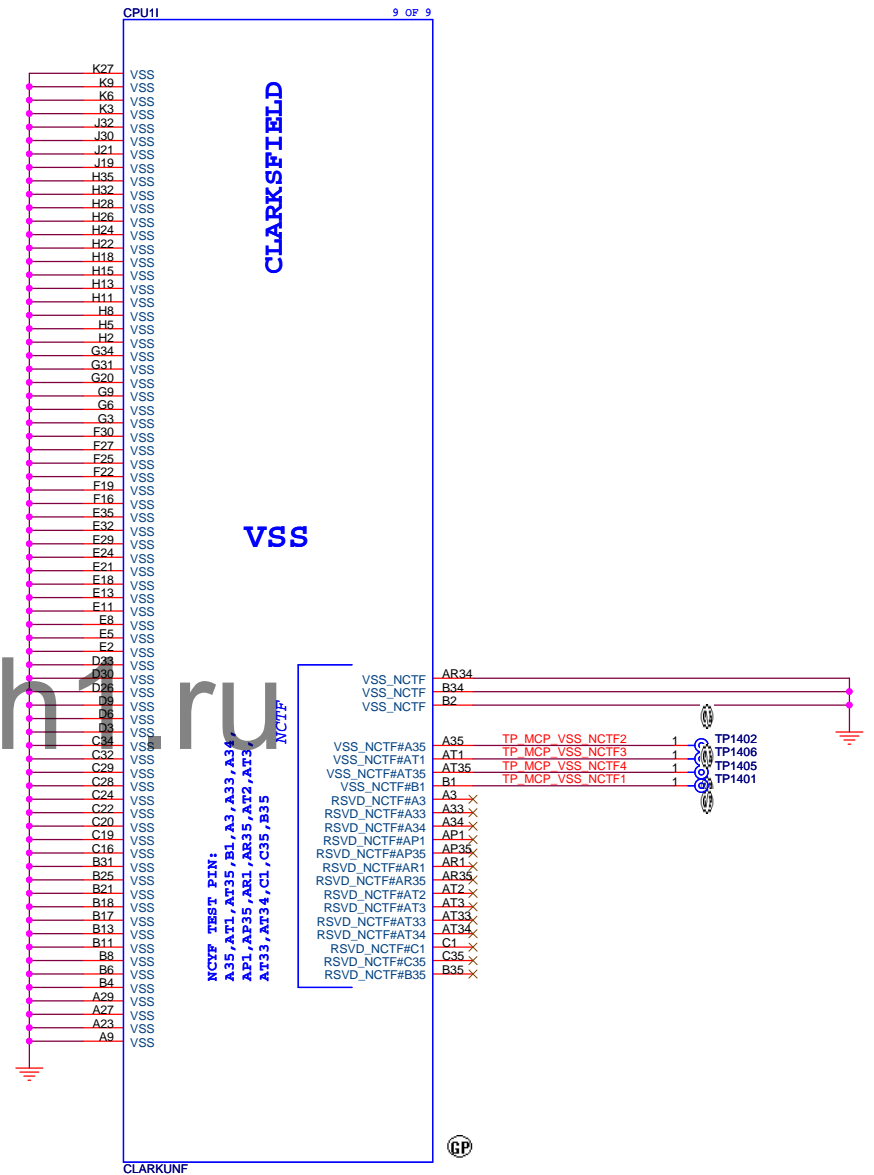
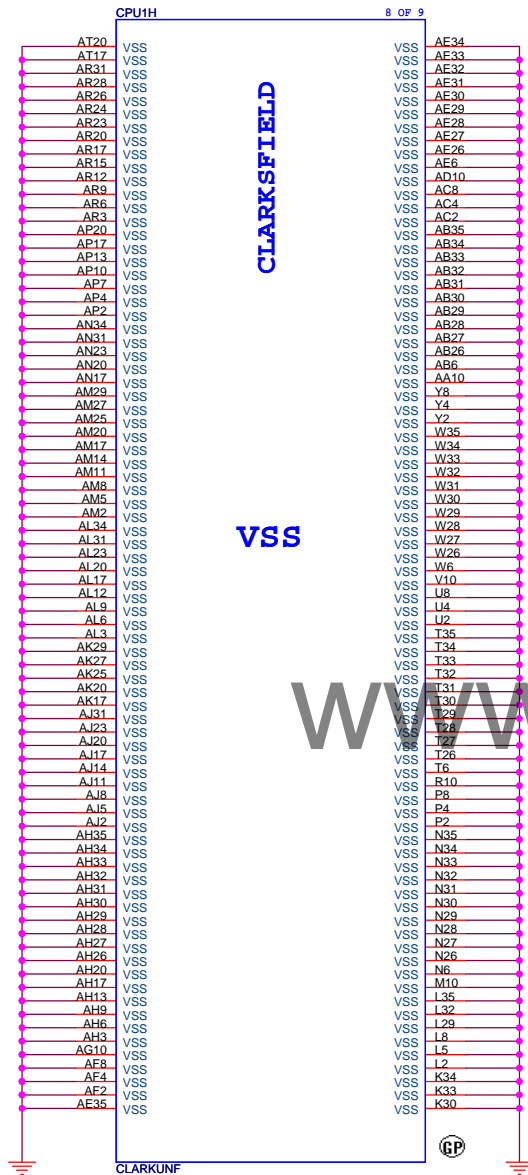
VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

<Core Design>



Title			
CPU (RESERVED)			
Size	Document Number	Rev	
Date: Monday, January 18, 2010	Sheet 11	of 91	Rev X01





<Core Design>




Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
CPU (VSS)			
Size	Document Number		Rev
	Vostro Calpella		X01
Date:	Monday, January 18, 2010	Sheet 14 of	91

(Blanking)

www.aitech1.ru

<Core Design>



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved


Size A3	Document Number Vostro Calpella	Rev X01
------------	---	-------------------

Date: Monday, January 18, 2010	Sheet 15 of 91
--------------------------------	----------------

(Blanking)

www.aitech1.ru

<Core Design>



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved


Size A3	Document Number Vostro Calpella	Rev X01
------------	---	-------------------

Date: Monday, January 18, 2010	Sheet 16 of 91
--------------------------------	----------------

(Blank)

www.aitech1.ru

<Core Design>



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

File

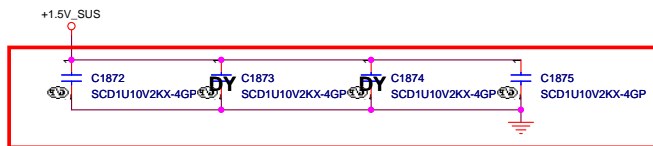
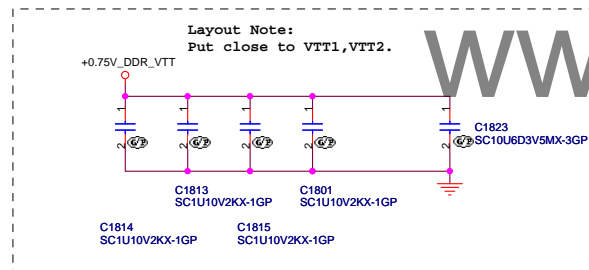
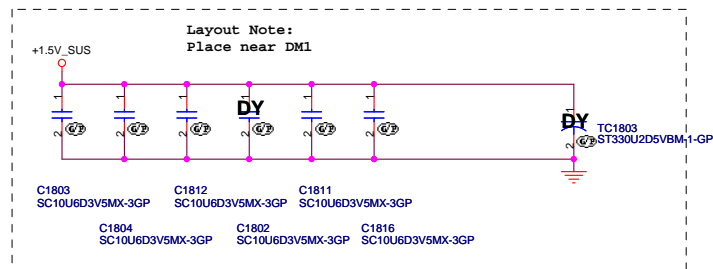
(Reserve)

Size	Document Number	Rev
Custom	Vostro Calpella	X01

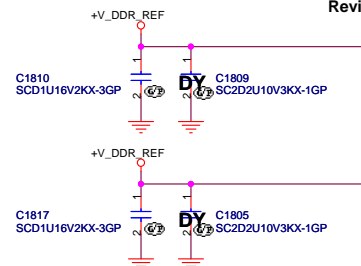
Date: Monday, January 18, 2010	Sheet 17 of 91
--------------------------------	----------------

SSID = MEMORY

[10] M_A_DQS#[7..0] << >>
[10] M_A_DQ[63..0] << >>
[10] M_A_DM[7..0] << >>
[10] M_A_DQS[7..0] << >>
[10] M_A_A[15..0] << >>



425302_425302_Calpella_S3PowerReduction_WhitePape
Revision 0.7



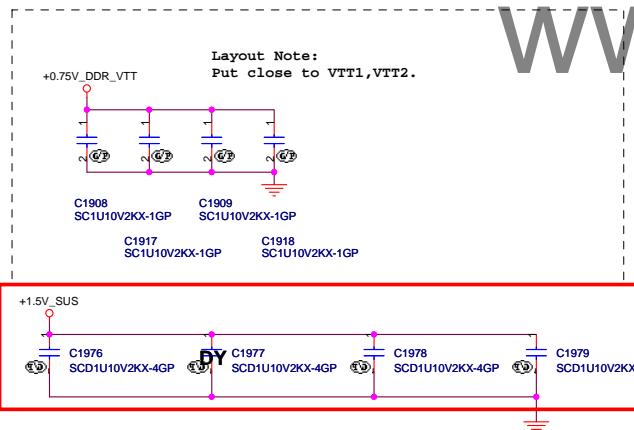
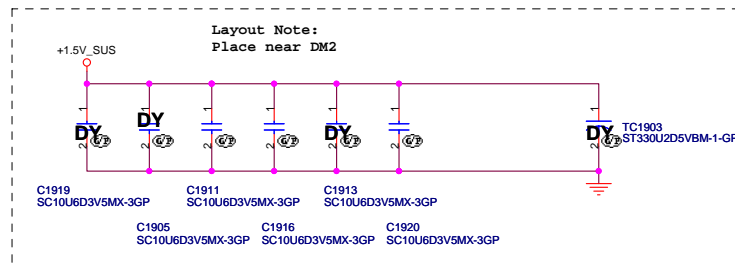
[10] M_ODT0 << >>
[10] M_ODT1 << >>
[9,19] DDR3_DRAMRST# << >>

M_A A0	98	A0	NP1	NP1
M_A A1	97	A1	NP2	NP2
M_A A2	96	A2		
M_A A3	95	A3		
M_A A4	94	A4		
M_A A5	93	A5		
M_A A6	92	A6		
M_A A7	91	A7		
M_A A8	90	A8		
M_A A9	89	A9		
M_A A10	88	A10/AP		
M_A A11	87	A11		
M_A A12	86	A12		
M_A A13	85	A13		
M_A A14	84	A14		
M_A A15	83	A15		
M_A BS2	82	A16/BA2		
M_A BS0	81	BA0		
M_A BS1	80	BA1		
M_A DQ0	79	DQ0		
M_A DQ1	78	DQ1		
M_A DQ2	77	DQ2		
M_A DQ3	76	DQ3		
M_A DQ4	75	DQ4		
M_A DQ5	74	DQ5		
M_A DQ6	73	DQ6		
M_A DQ7	72	DQ7		
M_A DQ8	71	DQ8		
M_A DQ9	70	DQ9		
M_A DQ10	69	DQ10		
M_A DQ11	68	DQ11		
M_A DQ12	67	DQ12		
M_A DQ13	66	DQ13		
M_A DQ14	65	DQ14		
M_A DQ15	64	DQ15		
M_A DQ16	63	DQ16		
M_A DQ17	62	DQ17		
M_A DQ18	61	DQ18		
M_A DQ19	60	DQ19		
M_A DQ20	59	DQ20		
M_A DQ21	58	DQ21		
M_A DQ22	57	DQ22		
M_A DQ23	56	DQ23		
M_A DQ24	55	DQ24		
M_A DQ25	54	DQ25		
M_A DQ26	53	DQ26		
M_A DQ27	52	DQ27		
M_A DQ28	51	DQ28		
M_A DQ29	50	DQ29		
M_A DQ30	49	DQ30		
M_A DQ31	48	DQ31		
M_A DQ32	47	DQ32		
M_A DQ33	46	DQ33		
M_A DQ34	45	DQ34		
M_A DQ35	44	DQ35		
M_A DQ36	43	DQ36		
M_A DQ37	42	DQ37		
M_A DQ38	41	DQ38		
M_A DQ39	40	DQ39		
M_A DQ40	39	DQ40		
M_A DQ41	38	DQ41		
M_A DQ42	37	DQ42		
M_A DQ43	36	DQ43		
M_A DQ44	35	DQ44		
M_A DQ45	34	DQ45		
M_A DQ46	33	DQ46		
M_A DQ47	32	DQ47		
M_A DQ48	31	DQ48		
M_A DQ49	30	DQ49		
M_A DQ50	29	DQ50		
M_A DQ51	28	DQ51		
M_A DQ52	27	DQ52		
M_A DQ53	26	DQ53		
M_A DQ54	25	DQ54		
M_A DQ55	24	DQ55		
M_A DQ56	23	DQ56		
M_A DQ57	22	DQ57		
M_A DQ58	21	DQ58		
M_A DQ59	20	DQ59		
M_A DQ60	19	DQ60		
M_A DQ61	18	DQ61		
M_A DQ62	17	DQ62		
M_A DQ63	16	DQ63		
M_A DQS#0	15	DQS#0		
M_A DQS#1	14	DQS#1		
M_A DQS#2	13	DQS#2		
M_A DQS#3	12	DQS#3		
M_A DQS#4	11	DQS#4		
M_A DQS#5	10	DQS#5		
M_A DQS#6	9	DQS#6		
M_A DQS#7	8	DQS#7		
M_A DQS#8	7	DQS#8		
M_A DQS#9	6	DQS#9		
M_A DQS#10	5	DQS#10		
M_A DQS#11	4	DQS#11		
M_A DQS#12	3	DQS#12		
M_A DQS#13	2	DQS#13		
M_A DQS#14	1	DQS#14		
M_A DQS#15	0	DQS#15		
M_A DQS#16	0	DQS#16		
M_A DQS#17	0	DQS#17		
M_A DQS#18	0	DQS#18		
M_A DQS#19	0	DQS#19		
M_A DQS#20	0	DQS#20		
M_A DQS#21	0	DQS#21		
M_A DQS#22	0	DQS#22		
M_A DQS#23	0	DQS#23		
M_A DQS#24	0	DQS#24		
M_A DQS#25	0	DQS#25		
M_A DQS#26	0	DQS#26		
M_A DQS#27	0	DQS#27		
M_A DQS#28	0	DQS#28		
M_A DQS#29	0	DQS#29		
M_A DQS#30	0	DQS#30		
M_A DQS#31	0	DQS#31		
M_A DQS#32	0	DQS#32		
M_A DQS#33	0	DQS#33		
M_A DQS#34	0	DQS#34		
M_A DQS#35	0	DQS#35		
M_A DQS#36	0	DQS#36		
M_A DQS#37	0	DQS#37		
M_A DQS#38	0	DQS#38		
M_A DQS#39	0	DQS#39		
M_A DQS#40	0	DQS#40		
M_A DQS#41	0	DQS#41		
M_A DQS#42	0	DQS#42		
M_A DQS#43	0	DQS#43		
M_A DQS#44	0	DQS#44		
M_A DQS#45	0	DQS#45		
M_A DQS#46	0	DQS#46		
M_A DQS#47	0	DQS#47		
M_A DQS#48	0	DQS#48		
M_A DQS#49	0	DQS#49		
M_A DQS#50	0	DQS#50		
M_A DQS#51	0	DQS#51		
M_A DQS#52	0	DQS#52		
M_A DQS#53	0	DQS#53		
M_A DQS#54	0	DQS#54		
M_A DQS#55	0	DQS#55		
M_A DQS#56	0	DQS#56		
M_A DQS#57	0	DQS#57		
M_A DQS#58	0	DQS#58		
M_A DQS#59	0	DQS#59		
M_A DQS#60	0	DQS#60		
M_A DQS#61	0	DQS#61		
M_A DQS#62	0	DQS#62		
M_A DQS#63	0	DQS#63		
M_A DQS#64	0	DQS#64		
M_A DQS#65	0	DQS#65		
M_A DQS#66	0	DQS#66		
M_A DQS#67	0	DQS#67		
M_A DQS#68	0	DQS#68		
M_A DQS#69	0	DQS#69		
M_A DQS#70	0	DQS#70		
M_A DQS#71	0	DQS#71		
M_A DQS#72	0	DQS#72		
M_A DQS#73	0	DQS#73		
M_A DQS#74	0	DQS#74		
M_A DQS#75	0	DQS#75		
M_A DQS#76	0	DQS#76		
M_A DQS#77	0	DQS#77		
M_A DQS#78	0	DQS#78		
M_A DQS#79	0	DQS#79		
M_A DQS#80	0	DQS#80		
M_A DQS#81	0	DQS#81		
M_A DQS#82	0	DQS#82		
M_A DQS#83	0	DQS#83		
M_A DQS#84	0	DQS#84		
M_A DQS#85	0	DQS#85		
M_A DQS#86	0	DQS#86		
M_A DQS#87	0	DQS#87		
M_A DQS#88	0	DQS#88		
M_A DQS#89	0	DQS#89		
M_A DQS#90	0	DQS#90		
M_A DQS#91	0	DQS#91		
M_A DQS#92	0	DQS#92		
M_A DQS#93	0	DQS#93		
M_A DQS#94	0	DQS#94		
M_A DQS#95	0	DQS#95		
M_A DQS#96	0	DQS#96		
M_A DQS#97	0	DQS#97		
M_A DQS#98	0	DQS#98		
M_A DQS#99	0	DQS#99		
M_A DQS#100	0	DQS#100		
M_A DQS#101	0	DQS#101		
M_A DQS#102	0	DQS#102		
M_A DQS#103	0	DQS#103		
M_A DQS#104	0	DQS#104		
M_A DQS#105	0	DQS#105		
M_A DQS#106	0	DQS#106		
M_A DQS#107	0	DQS#107		
M_A DQS#108	0	DQS#108		
M_A DQS#109	0	DQS#109		
M_A DQS#110	0	DQS#110		
M_A DQS#111	0	DQS#111		
M_A DQS#112	0	DQS#112		
M_A DQS#113	0	DQS#113		
M_A DQS#114	0	DQS#114		
M_A DQS#115	0	DQS#115		
M_A DQS#116	0	DQS#116		
M_A DQS#117	0	DQS#117		
M_A DQS#118	0	DQS#118		
M_A DQS#119	0	DQS#119		
M_A DQS#120	0	DQS#120		
M_A DQS#121	0	DQS#121		
M_A DQS#122	0	DQS#122		
M_A DQS#123	0	DQS#123		
M_A DQS#124	0	DQS#124		
M_A DQS#125	0	DQS#125		
M_A DQS#126	0	DQS#126		
M_A DQS#127	0	DQS#127		
M_A DQS#128	0	DQS#128		
M_A DQS#129	0	DQS#129		
M_A DQS#130	0	DQS#130		
M_A DQS#131	0	DQS#131		
M_A DQS#132	0	DQS#132		
M_A DQS#133	0	DQS#133		
M_A DQS#134	0	DQS#134		
M_A DQS#135	0	DQS#135		
M_A DQS#136	0	DQS#136		
M_A DQS#137	0	DQS#137		
M_A DQS#138	0	DQS#138		
M_A DQS#139	0	DQS#139		
M_A DQS#140	0	DQS#140		
M_A DQS#141	0	DQS#141		
M_A DQS#142	0	DQS#142		
M_A DQS#143	0	DQS#143		
M_A DQS#144	0	DQS#144		
M_A DQS#145	0	DQS#145		
M_A DQS#146	0	DQS#146		
M_A DQS#147	0	DQS#147		
M_A DQS#148	0	DQS#148		
M_A DQS#149	0	DQS#149		
M_A DQS#150	0	DQS#150		
M_A DQS#151	0	DQS#151		
M_A DQS#152	0	DQS#152		
M_A DQS#153	0	DQS#153		
M_A DQS#154	0	DQS#154		
M_A DQS#155	0	DQS#155		
M_A DQS#156	0	DQS#156		
M_A DQS#157	0	DQS#157		
M_A DQS#158	0	DQS#158		
M_A DQS#159	0	DQS#159		
M_A DQS#160	0	DQS#160		
M_A DQS#161	0	DQS#161		
M_A DQS#162	0	DQS#162		
M_A DQS#163	0	DQS#163		
M_A DQS#164	0	DQS#164		
M_A DQS#165	0	DQS#165		
M_A DQS#166	0	DQS#166		
M_A DQS#167	0	DQS#167		
M_A DQS#168	0	DQS#168		
M_A DQS#169	0	DQS#169		
M_A DQS#170	0	DQS#170		
M_A DQS#171	0	DQS#171		
M_A DQS#172	0	DQS#172		
M_A DQS#173	0	DQS#173		
M_A DQS#174	0	DQS#174		
M_A DQS#175	0	DQS#175		
M_A DQS#176	0	DQS#176		
M_A DQS#177	0	DQS#177		
M_A DQS#178	0	DQS#178		
M_A DQS#179	0	DQS#179		
M_A DQS#180	0	DQS#180		
M_A DQS#181	0	DQS#181		
M_A DQS#182	0	DQS#182		
M_A DQS#183	0	DQS#183		
M_A DQS#184	0	DQS#184		
M_A DQS#185	0	DQS#185		
M_A DQS#186	0	DQS#186		
M_A DQS#187	0	DQS#187		
M_A DQS#188	0	DQS#188		
M_A DQS#189	0	DQS#189		
M_A DQS#190	0	DQS#190		
M_A DQS#191	0	DQS#191		
M_A DQS#192	0	DQS#192		
M_A DQS#193	0	DQS#193		
M_A DQS#194	0	DQS#194		
M_A DQS#195	0	DQS#195		
M_A DQS#196	0	DQS#196		
M_A DQS#197	0	DQS#197		
M_A DQS#198	0	DQS#198		
M_A DQS#199	0	DQS#199		
M_A DQS#200	0	DQS#200		
M_A DQS#201	0	DQS#201		
M_A DQS#202	0	DQS#202		
M_A DQS#203	0	DQS#203		
M_A DQS#204	0	DQS#204		
M_A DQS#205	0	DQS#205		
M_A DQS#206	0	DQS#206		
M_A DQS#207	0	DQS#207		
M_A DQS#208	0	DQS#208		
M_A DQS#209	0	DQS#209		

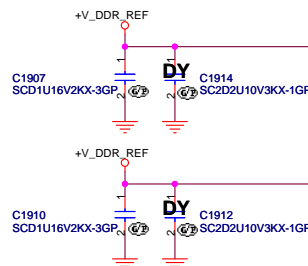
SSID = MEMORY

[10] M_B_DQS# [7..0] << >>
 [10] M_B_DQ [63..0] << >>
 [10] M_B_DM [7..0] << >>
 [10] M_B_DQS [7..0] << >>
 [10] M_B_A [15..0] << >>

[10] M_B_BS2 >>>
 [10] M_B_BS0 >>>
 [10] M_B_BS1 >>>



425302_425302_Calpella_S3PowerReduction_WhitePage
 Revision 0.7



[10] M_ODT2 >>>
 [10] M_ODT3 >>>

[9,18] DDR3_DRAMRST# >>>

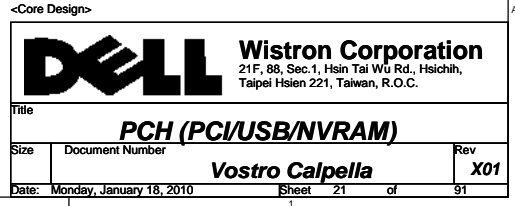
M_B A0	98	A0	NP1
M_B A1	97	A1	NP2
M_B A2	96	A2	
M_B A3	95	A3	
M_B A4	92	A4	
M_B A5	91	A5	
M_B A6	90	A6	
M_B A7	86	A7	
M_B A8	89	A8	
M_B A9	85	A9	
M_B A10	107	A10/AP	
M_B A11	84	A11	
M_B A12	83	A12	
M_B A13	119	A13	
M_B A14	80	A14	
M_B A15	78	A15	
M_B BS2	79	A16/BA2	
M_B BS0	109	BA0	
M_B BS1	108	BA1	
M_B DQ0	5	DQ0	
M_B DQ1	7	DQ1	
M_B DQ2	15	DQ2	
M_B DQ3	17	DQ3	
M_B DQ4	4	DQ4	
M_B DQ5	16	DQ5	
M_B DQ6	18	DQ6	
M_B DQ7	21	DQ7	
M_B DQ8	23	DQ8	
M_B DQ9	33	DQ9	
M_B DQ10	35	DQ10	
M_B DQ11	22	DQ11	
M_B DQ12	24	DQ12	
M_B DQ13	34	DQ13	
M_B DQ14	36	DQ14	
M_B DQ15	39	DQ15	
M_B DQ16	41	DQ16	
M_B DQ17	51	DQ17	
M_B DQ18	53	DQ18	
M_B DQ19	40	DQ19	
M_B DQ20	42	DQ20	
M_B DQ21	50	DQ21	
M_B DQ22	52	DQ22	
M_B DQ23	57	DQ23	
M_B DQ24	59	DQ24	
M_B DQ25	67	DQ25	
M_B DQ26	69	DQ26	
M_B DQ27	56	DQ27	
M_B DQ28	58	DQ28	
M_B DQ29	68	DQ29	
M_B DQ30	70	DQ30	
M_B DQ31	129	DQ31	
M_B DQ32	131	DQ32	
M_B DQ33	141	DQ33	
M_B DQ34	143	DQ34	
M_B DQ35	130	DQ35	
M_B DQ36	132	DQ36	
M_B DQ37	140	DQ37	
M_B DQ38	142	DQ38	
M_B DQ39	147	DQ39	
M_B DQ40	149	DQ40	
M_B DQ41	157	DQ41	
M_B DQ42	159	DQ42	
M_B DQ43	146	DQ43	
M_B DQ44	148	DQ44	
M_B DQ45	158	DQ45	
M_B DQ46	160	DQ46	
M_B DQ47	163	DQ47	
M_B DQ48	165	DQ48	
M_B DQ49	175	DQ49	
M_B DQ50	177	DQ50	
M_B DQ51	164	DQ51	
M_B DQ52	166	DQ52	
M_B DQ53	174	DQ53	
M_B DQ54	176	DQ54	
M_B DQ55	181	DQ55	
M_B DQ56	183	DQ56	
M_B DQ57	191	DQ57	
M_B DQ58	193	DQ58	
M_B DQ59	180	DQ59	
M_B DQ60	182	DQ60	
M_B DQ61	192	DQ61	
M_B DQ62	194	DQ62	
M_B DQ63		DQ63	
M_B DQS#0	10	DQS0#	
M_B DQS#1	21	DQS1#	
M_B DQS#2	45	DQS2#	
M_B DQS#3	62	DQS3#	
M_B DQS#4	135	DQS4#	
M_B DQS#5	152	DQS5#	
M_B DQS#6	168	DQS6#	
M_B DQS#7	186	DQS7#	
M_B DQSO	12	DQSO	
M_B DQS1	29	DQS1	
M_B DQS2	47	DQS2	
M_B DQS3	64	DQS3	
M_B DQS4	137	DQS4	
M_B DQS5	154	DQS5	
M_B DQS6	171	DQS6	
M_B DQS7	188	DQS7	
M_B DQSO	116	DQSO	
M_B DQS1	120	DQS1	
M_B DQS2	126	DQS2	
M_B DQS3	1	DQS3	
M_B DQS4	30	DQS4	
M_B DQS5	203	DQS5	
M_B DQS6	204	DQS6	
M_B DQS7		DQS7	

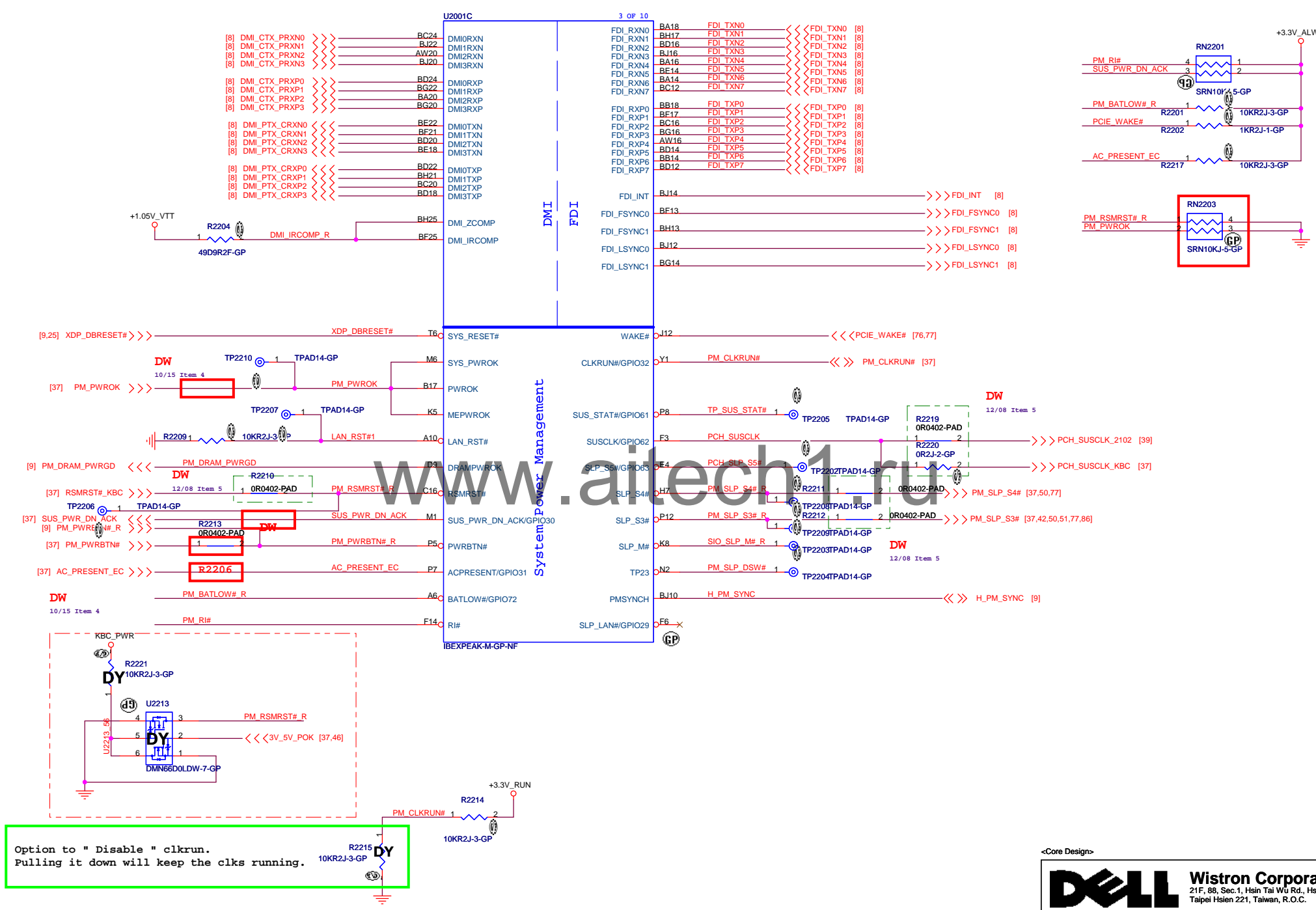
Height 9.2mm

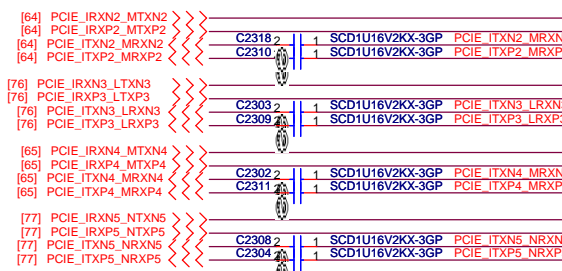
NP1	NP1		
NP2	NP2		
RAS#	110	<<<	M_B_RAS# [10]
WE#	113	<<<	M_B_WE# [10]
CAS#	115	<<<	M_B_CAS# [10]
CS0#	114	<<<	M_CS2# [10]
CS1#	121	<<<	M_CS3# [10]
CKE0	73	<<<	M_CKE2 [10]
CKE1	74	<<<	M_CKE3 [10]
CK0#	101	M_CLK_DDR2	M_CLK_DDR2 [10]
CK0#	103	M_CLK_DDR#2	M_CLK_DDR#2 [10]
CK1#	102	M_CLK_DDR3	M_CLK_DDR3 [10]
CK1#	104	M_CLK_DDR#3	M_CLK_DDR#3 [10]
DM0	11	M_B_DM0	
DM1	28	M_B_DM1	
DM2	46	M_B_DM2	
DM3	63	M_B_DM3	
DM4	136	M_B_DM4	
DM5	153	M_B_DM5	
DM6	170	M_B_DM6	
DM7	187	M_B_DM7	
SDA	200	PCH_SMBDATA	PCH_SMBDATA [7,18,23,40,64,65]
SCL	202	PCH_SMBCLK	PCH_SMBCLK [7,18,23,40,64,65]
EVENT#	198	<<<	PM_EXTT#1 [9]
DDSPD	199		
SA0	197	SA0_DM2	
SA1	201	SA1_DM2	
NC#1	77	X	
NC#2	122	X	
NC#TEST	125	X	
VDD1	75		
VDD2	76		
VDD3	81		
VDD4	82		
VDD5	87		
VDD6	88		
VDD7	93		
VDD8	94		
VDD9	99		
VDD10	100		
VDD11	105		
VDD12	106		
VDD13	111		
VDD14	112		
VDD15	117		
VDD16	118		
VDD17	123		
VDD18	124		
VSS	2		
VSS	3		
VSS	8		
VSS	9		
VSS	13		
VSS	14		
VSS	19		
VSS	20		
VSS	25		
VSS	26		
VSS	31		
VSS	32		
VSS	37		
VSS	38		
VSS	43		
VSS	44		
VSS	48		
VSS	49		
VSS	54		
VSS	55		
VSS	60		
VSS	61		
VSS	65		
VSS	66		
VSS	71		
VSS	72		
VSS	127		
VSS	128		
VSS	133		
VSS	134		
VSS	138		
VSS	139		
VSS	144		
VSS	145		
VSS	150		
VSS	151		
VSS	155		
VSS	156		
VSS	161		
VSS	162		
VSS	167		
VSS	168		
VSS	172		
VSS	173		
VSS	178		
VSS	179		
VSS	184		
VSS	185		
VSS	189		
VSS	190		
VSS	195		
VSS	196		
VSS	205		
VSS	206		

GP

62.10017.Q31



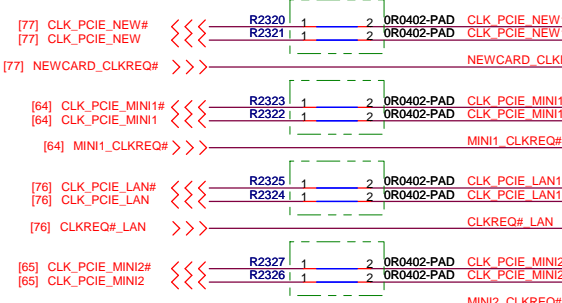




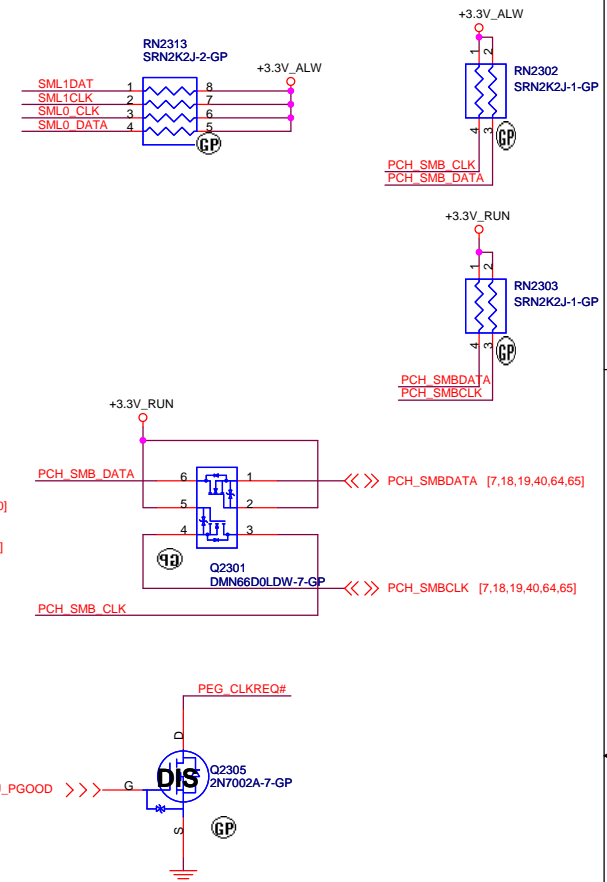
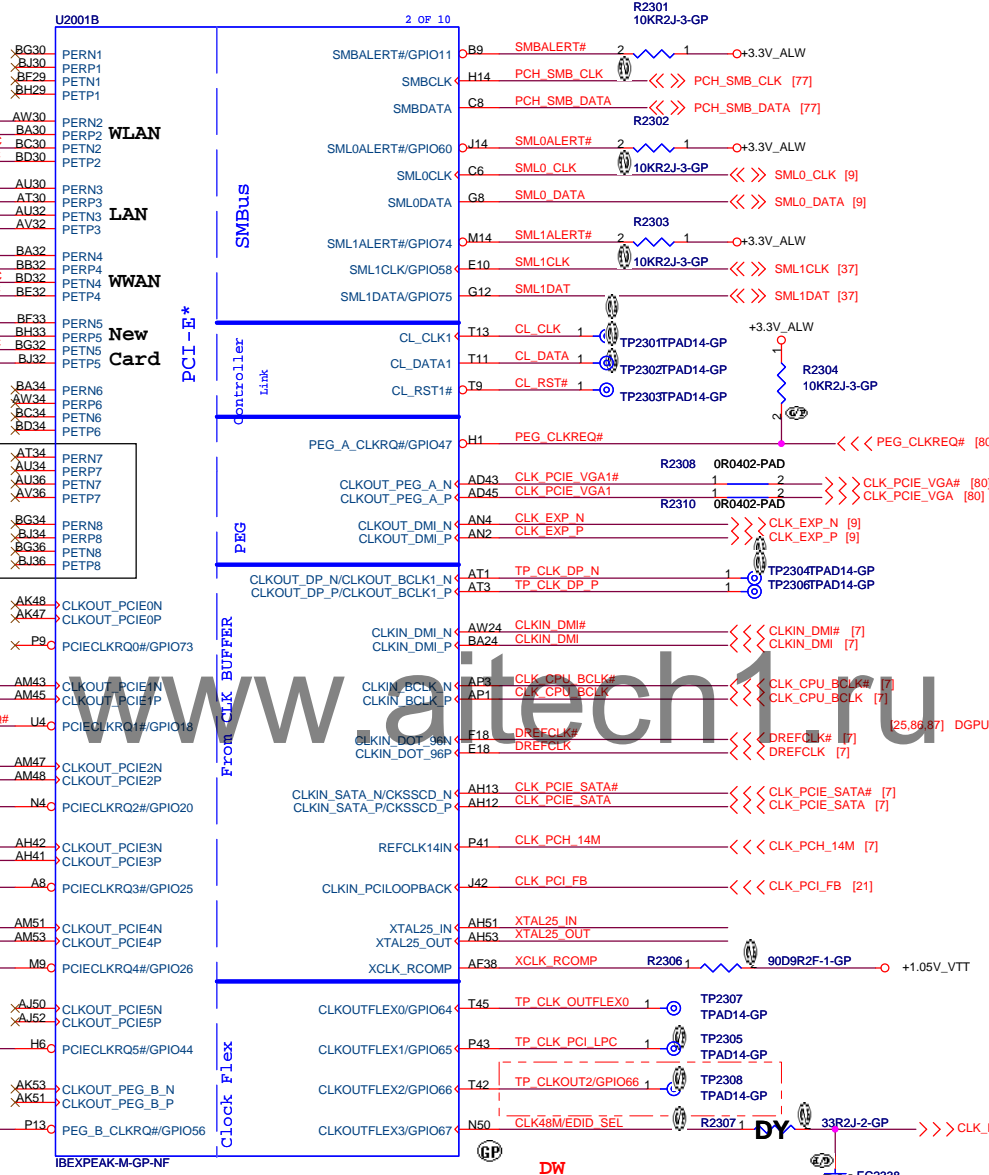
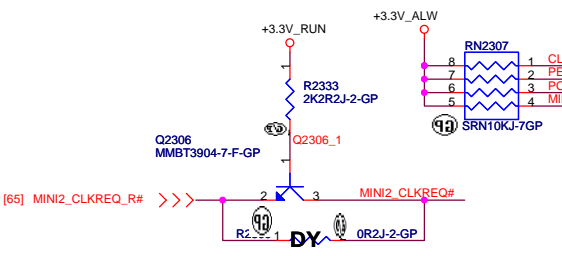
(Not available for HM55)

(Not available for HM55)

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3.3V_ALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +3.3_RUN



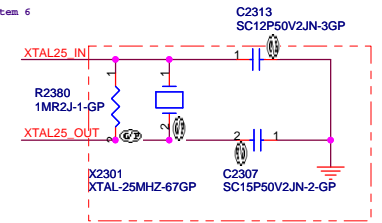
DW
12/10 Item 3
Reserve 0402 00hm resistors
, For RF Team to try solve PCIE noise



Display Clock Integration

	C2313	C2307	X2301	R2380
Normal	0R2J-2-GP	DY	DY	DY
dale DCI	SC18P	SC18P	25MHZ	1MR

DW
10/15 Item 6



Near R23071

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichu, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (PCI-E/SMBUS/CLOCK/CL)**

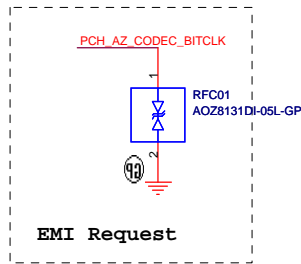
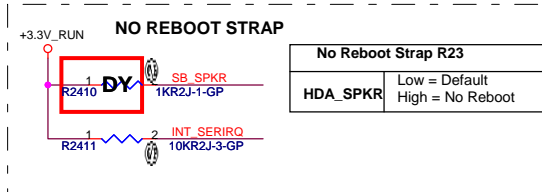
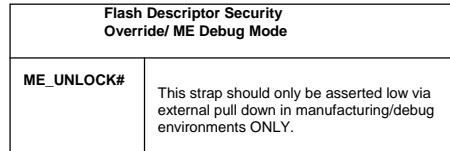
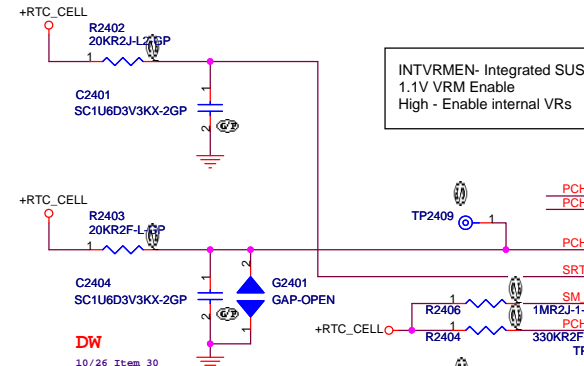
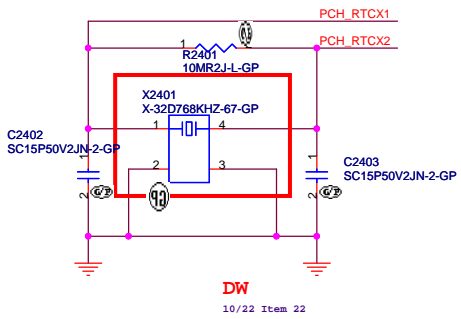
Size: Document Number

Date: Monday, January 18, 2010

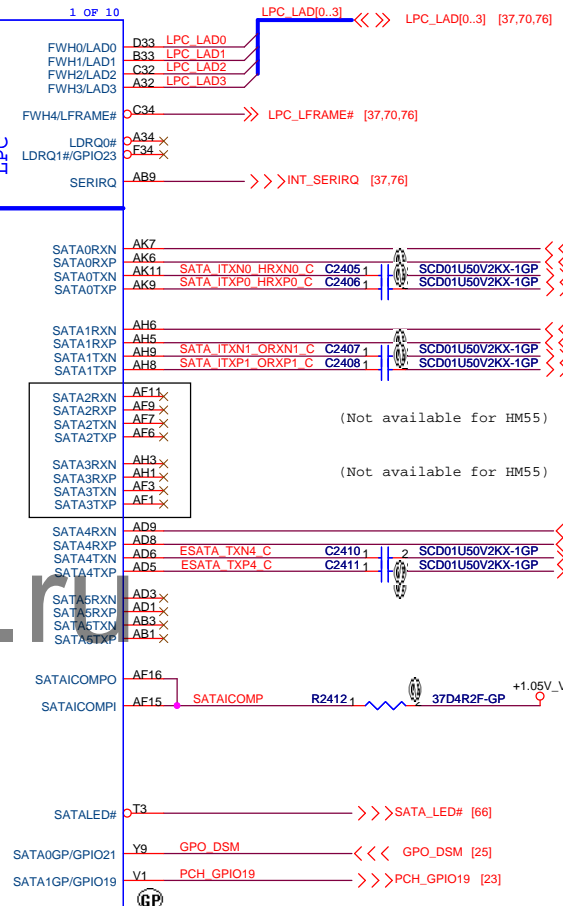
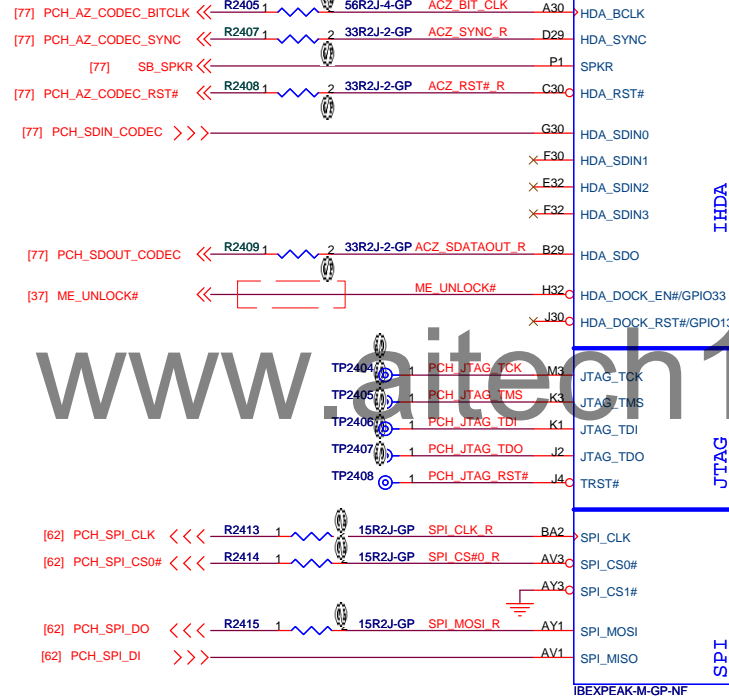
Rev: **X01**

Sheet: 23 of 91

Vostro Calpella



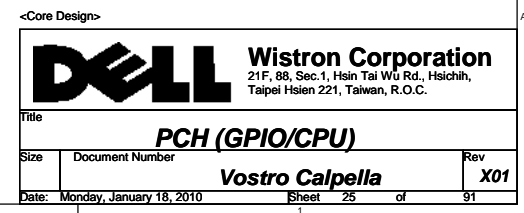
www.aitech1.net

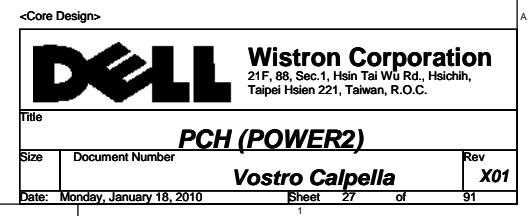


HDD

ODD

ESATA






(Blank)

www.aitech1.ru

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)


Size	Document Number	Rev
Custom	Vostro Calpella	X01

Date: Monday, January 18, 2010Sheet 29 of 91

(Blank)

www.aitech1.ru

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size	Document Number	Rev
Custom	Vostro Calpella	X01


Date: Monday, January 18, 2010	Sheet 30 of 91
--------------------------------	----------------

www.aitech1.ru

(Blank)

www.aitech1.ru

<Core Design>



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size

A3

Document Number

Vostro Calpella

Date: Monday, January 18, 2010

Sheet 32 of 91

Rev

X01

Reserve


(Blank)

www.aitech1.ru

(Blank)

www.aitech1.ru

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title


(Reserve)

Size	Document Number	Rev
Custom	Vostro Calpella	X01

Date: Monday, January 18, 2010	Sheet 34 of 91
--------------------------------	----------------

(Blank)
www.aitech1.ru

<Core Design>



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title


(Reserve)

Size A3	Document Number Vostro Calpella	Rev X01
------------	---	-------------------

Date: Monday, January 18, 2010	Sheet 35 of 91
--------------------------------	----------------

(Blank)
www.aitech1.ru

<Core Design>



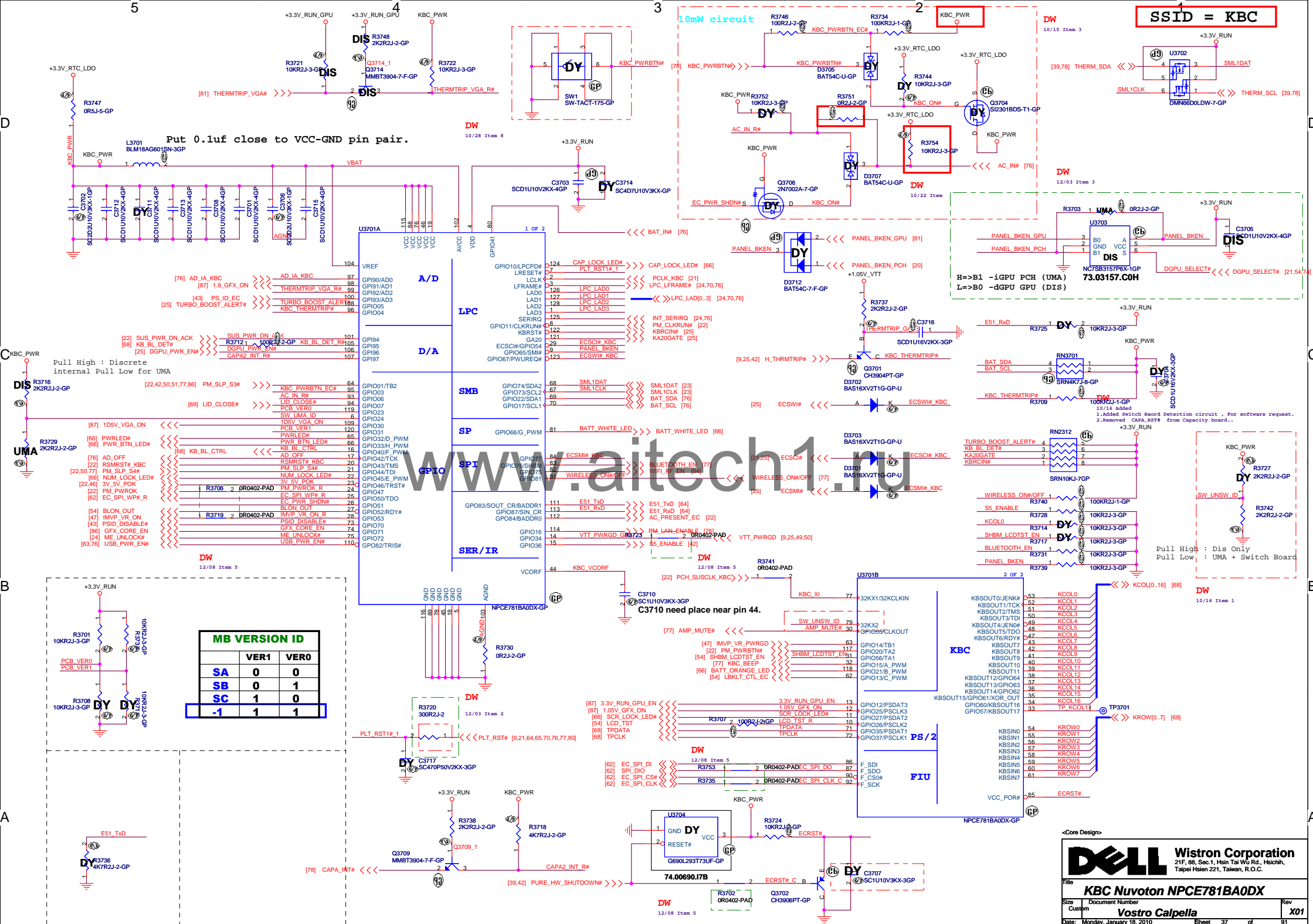
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)


Size A3	Document Number Vostro Calpella	Rev X01
------------	---	-------------------

Date: Monday, January 18, 2010	Sheet 36 of 91
--------------------------------	----------------



(Blank)
www.aitech1.ru

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

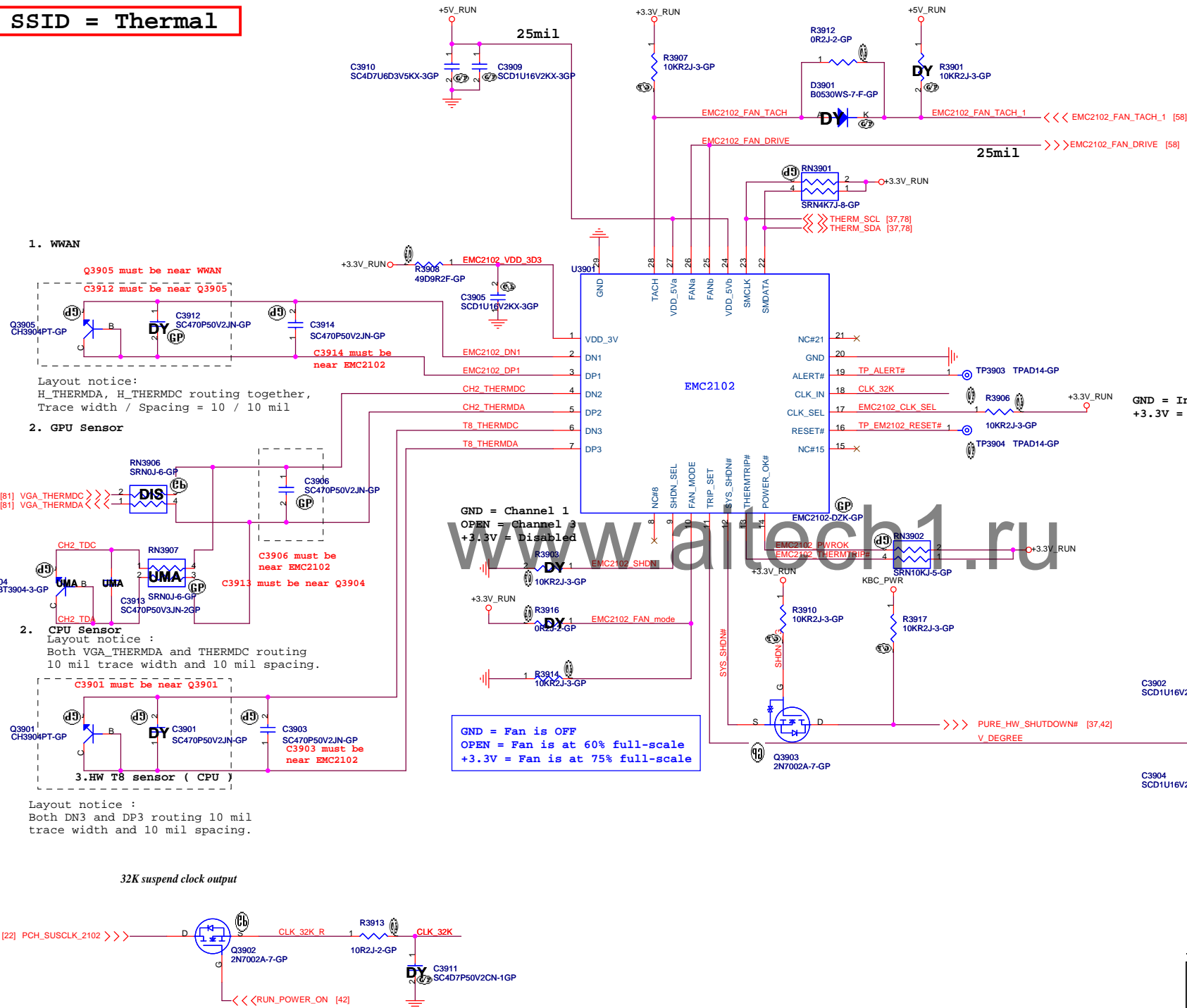
Title

(Reserve)

Size	Document Number	Rev
Custom	Vostro Calpella	X01

Date: Monday, January 18, 2010	Sheet 38 of 91
--------------------------------	----------------

SSID = Thermal



GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected

```
TRIP_SET Pin Voltage
V_DEGREE=((Degree-75)/21)
T8 shutdown is set 86 deg-C.
```

<Core Design>



(Blank)

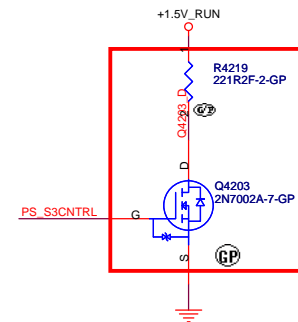
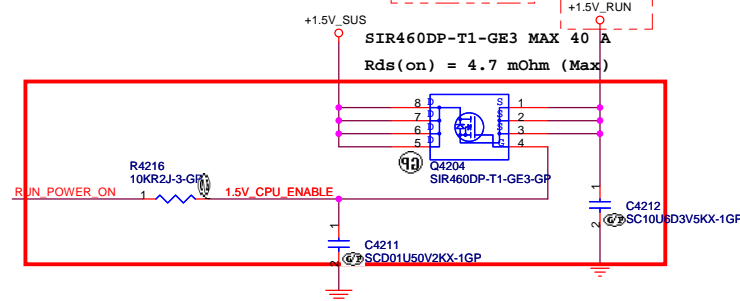
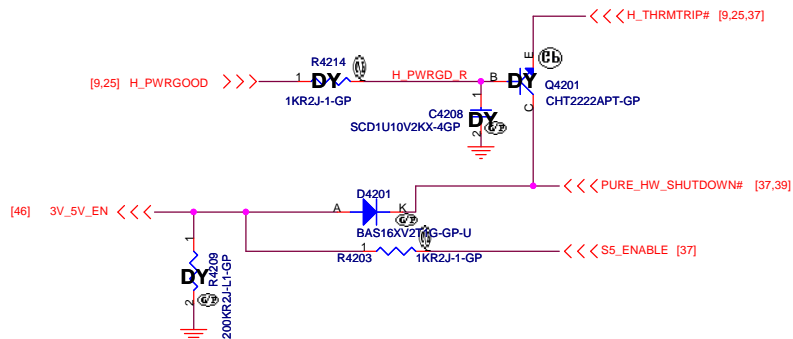
www.aitech1.ru

SSID = Reset.Suspend

+1.5V_RUN:

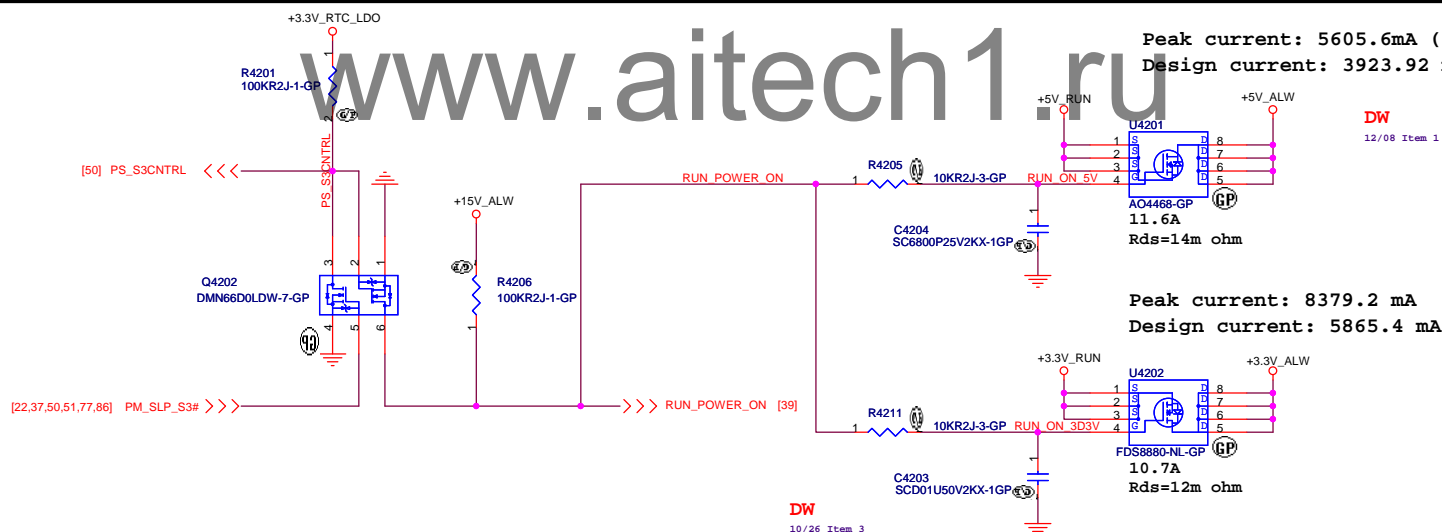
Peak current: 4650 mA

Design current: 3255 mA



Calpella Platform S3 Power Reduction Platform
S3 Power Reduction CRB Implementation
Design Details

Revision 0.1



Peak current: 5605.6mA (HD:1100 ODD:2500)

Design current: 3923.92 mA

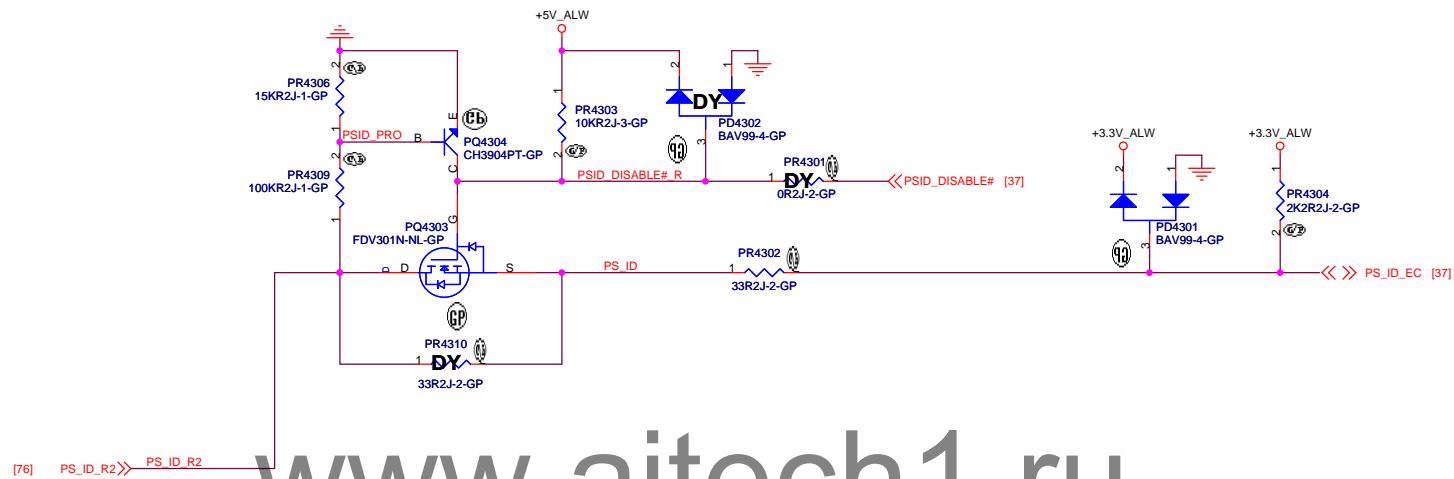
Peak current: 8379.2 mA
Design current: 5865.4 mA

DW
12/08 Item 1

DW
10/26 Item 3

<Core Design>

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Power Plane Enable			
Size	Document Number	Rev	
Custom	Vostro Calpella		X01
Date: Monday, January 18, 2010		Sheet 42	of 91




<Core Design>

(Blank)

www.aitech1.ru

<Core Design>



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title


(Reserve)

Size A3	Document Number Vostro Calpella	Rev X01
------------	---	-------------------

Date: Monday, January 18, 2010	Sheet 44 of 91
--------------------------------	----------------

(Blank)
www.aitech1.ru

<Core Design>



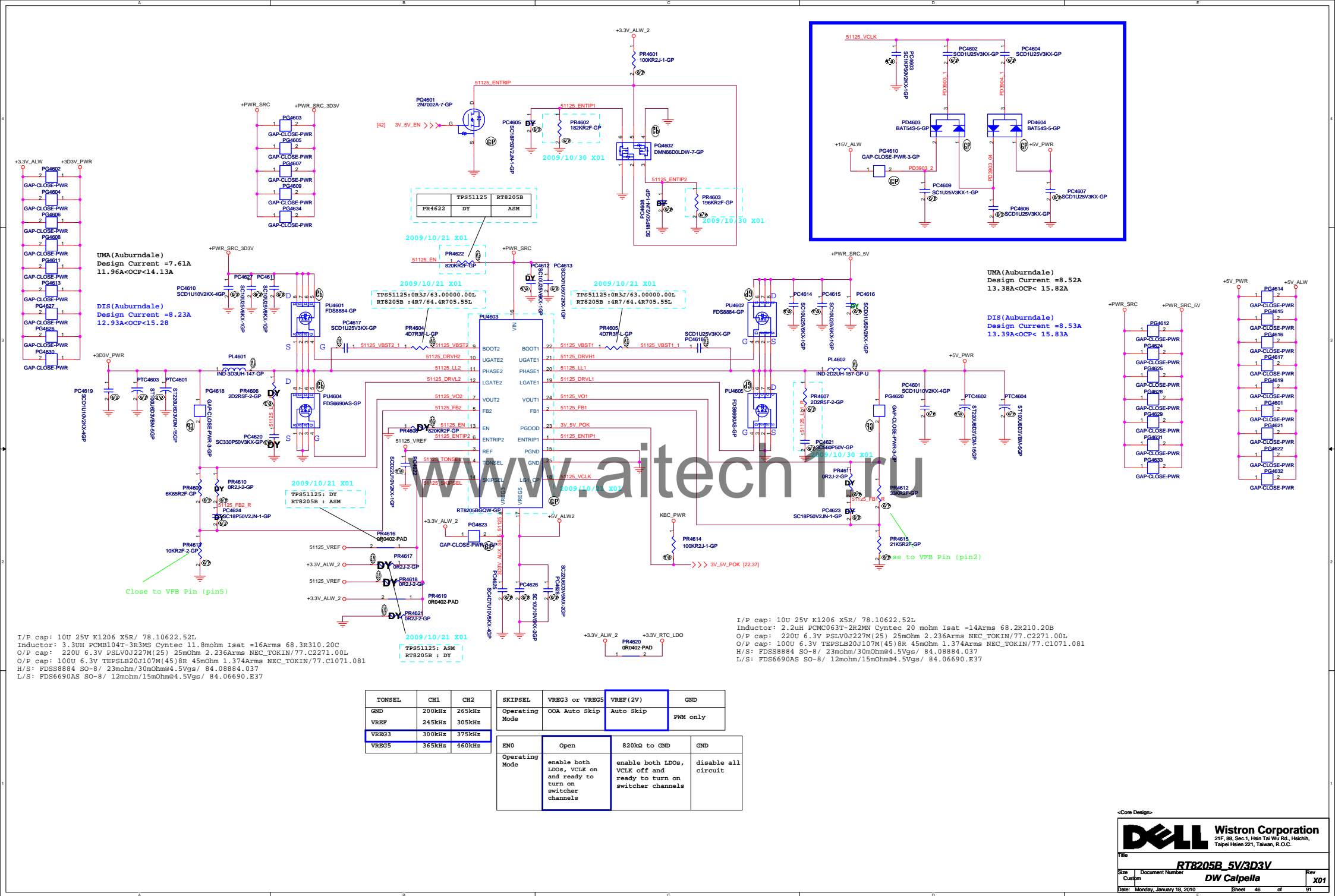
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size	Document Number	Rev
Custom	Vostro Calpella	X01

Date: Monday, January 18, 2010	Sheet 45 of 91
--------------------------------	----------------



UMA(Auburndale)
Design Current =7.61A
11.96A<OCP<14.13A

DIS(Auburndale)
Design Current =8.23A
12.93A<OCP<15.28

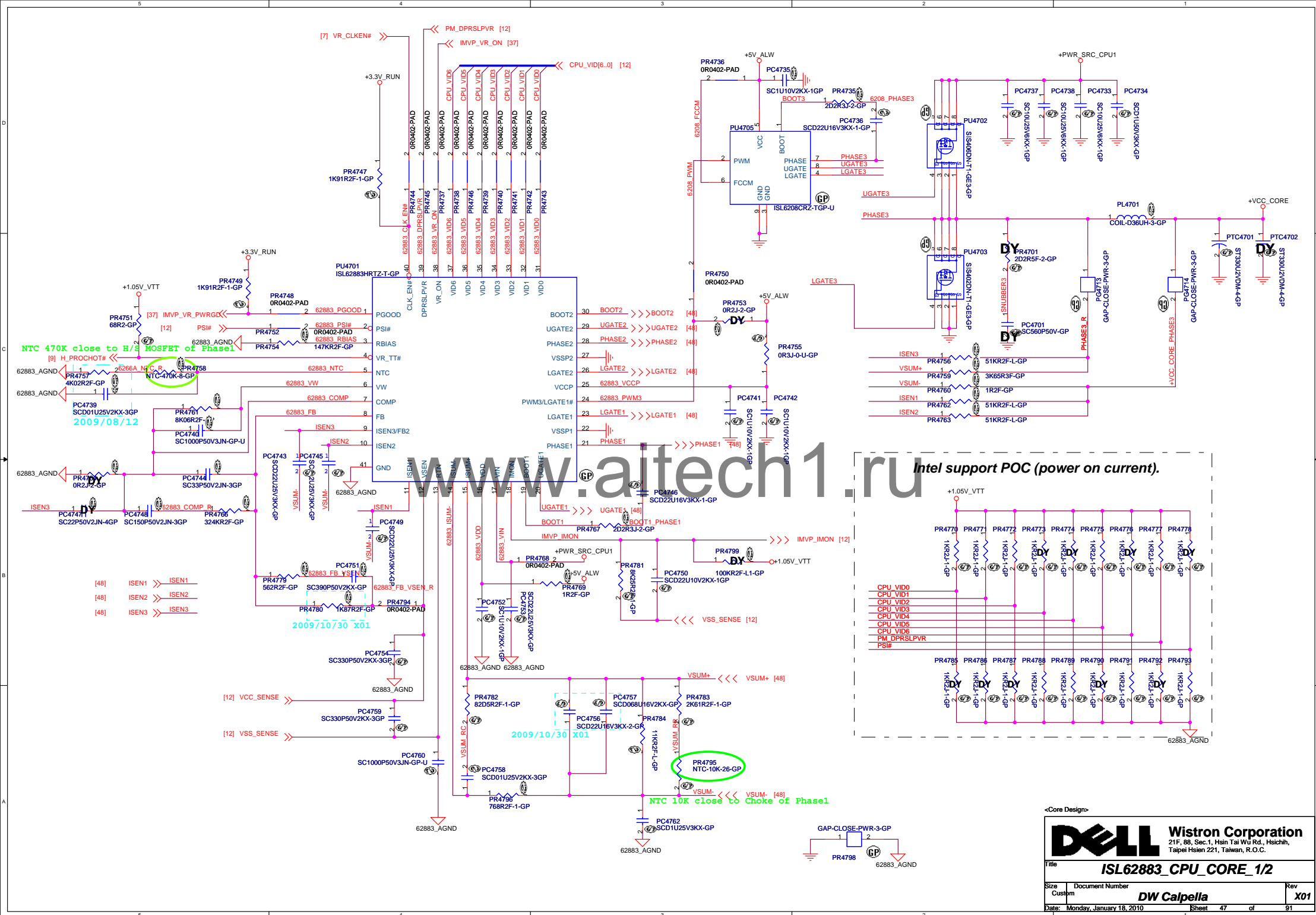
UMA(Auburndale)
Design Current =8.52A
13.38A<OCP< 15.82A

DIS(Auburndale)
Design Current =8.53A
13.39A<OCP< 15.83A

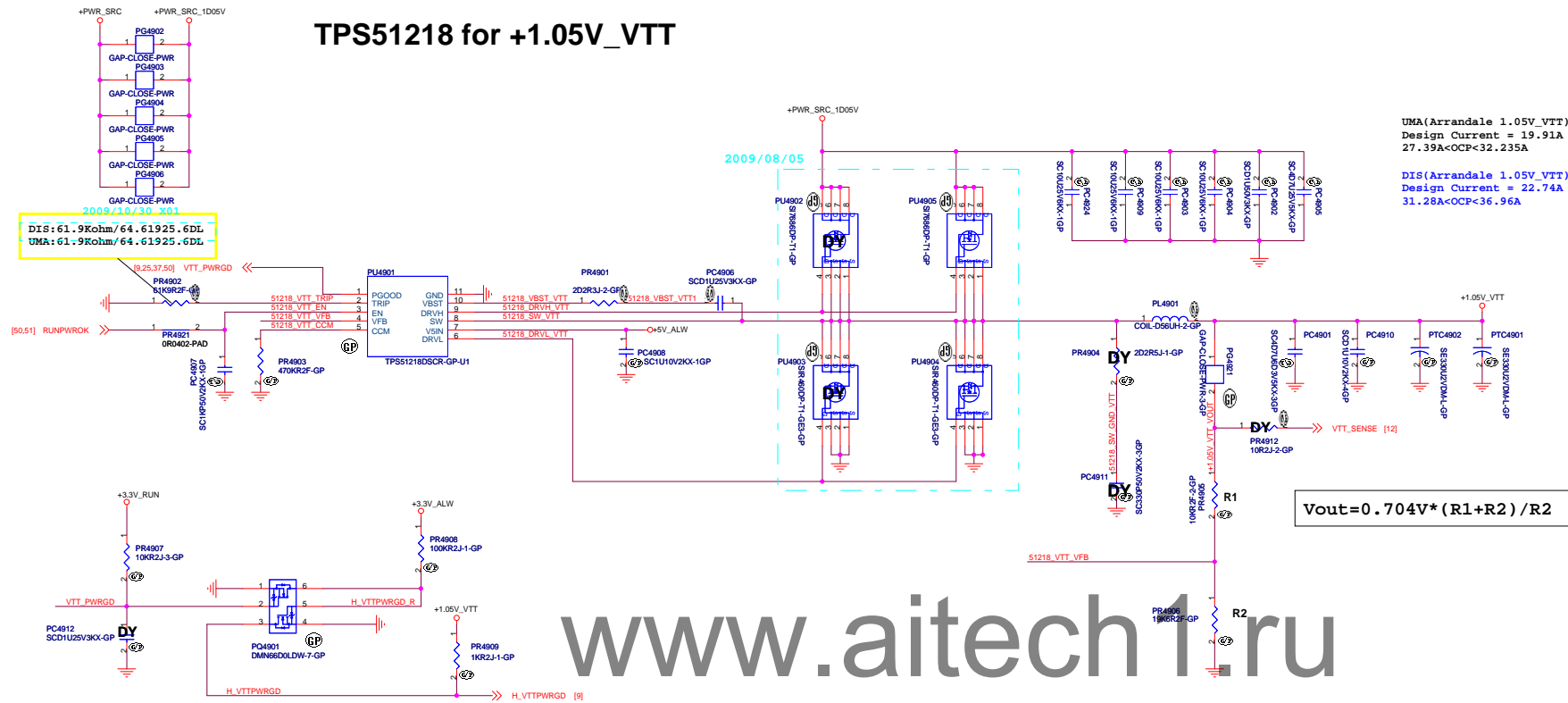
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH PCMB104T-3R3MS Cynotec 11.8mohm Isat =16Arms 68.3R310.20C
O/P cap: 220U 6.3V PSLV0J227M(25) 25mohm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mohm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDS58884 SO-8/ 23mohm/30mohm4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mohm4.5Vgs/ 84.06690.E37

TONSEL	CH1	CH2	SKIPSEL	VREG3 or VREG5	VREF (2V)	GND
GND	200kHz	265kHz	Operating Mode	OOA Auto Skip	Auto Skip	PWM only
VREF	245kHz	305kHz				
VREG3	300kHz	375kHz				
VREG5	365kHz	460kHz				

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit



TPS51218 for +1.05V_VTT

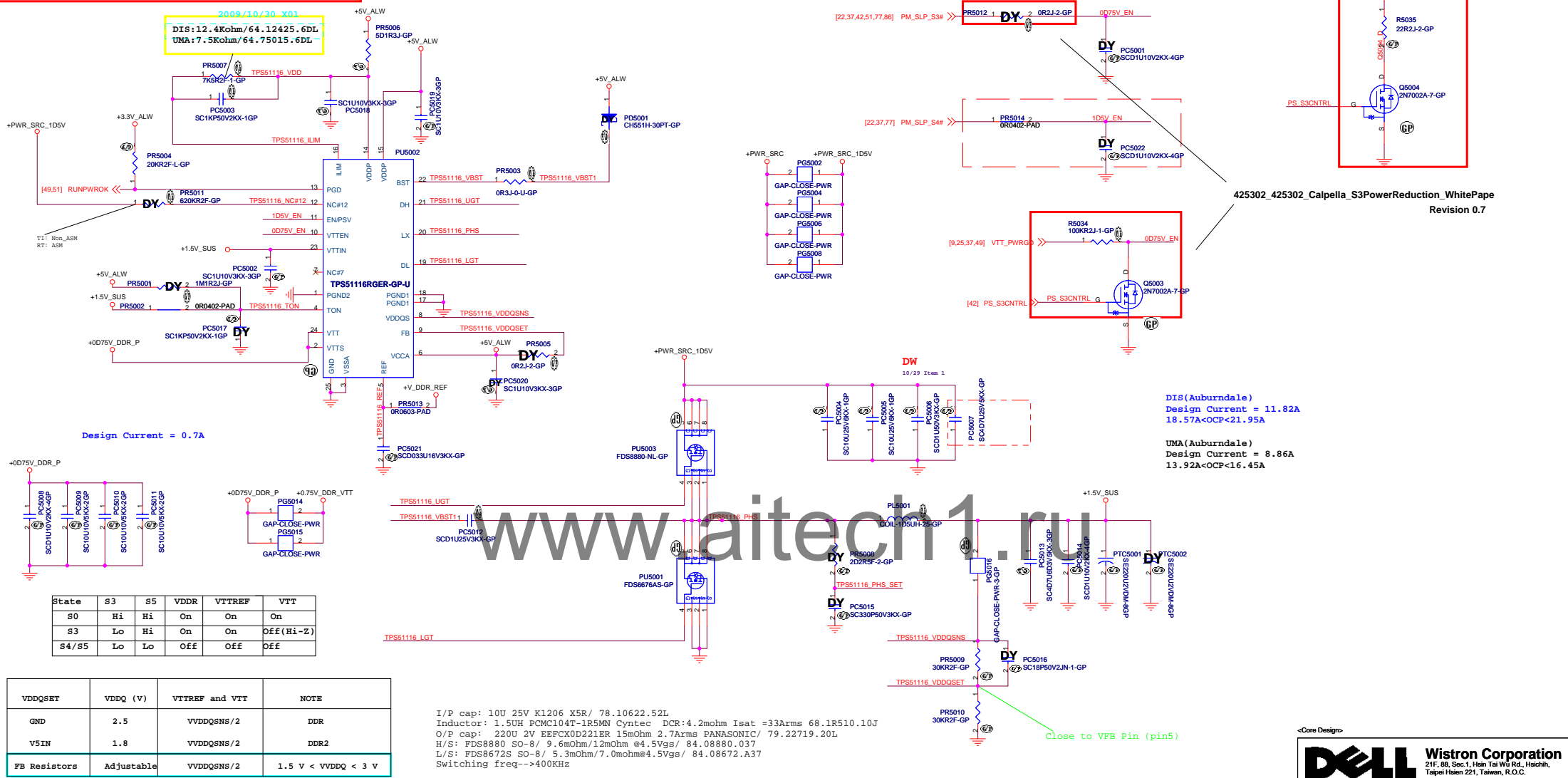


Frequency setting
470K -->290KHz
200K -->340KHz
100K -->380KHz
39K -->430KHz

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
H/S: SIR474DP-T1-GE3/10mohm/ 12mOhm@4.5Vgs/ 84.00474.037
L/S: SI7170DP-T1-GE3/3.6mOhm/4.3mohm@4.5Vgs/ 84.07170.037

<Core Design>

```
SSID = PWR.Plane.Regulator_1p5v0p75v
```



<Core Design>

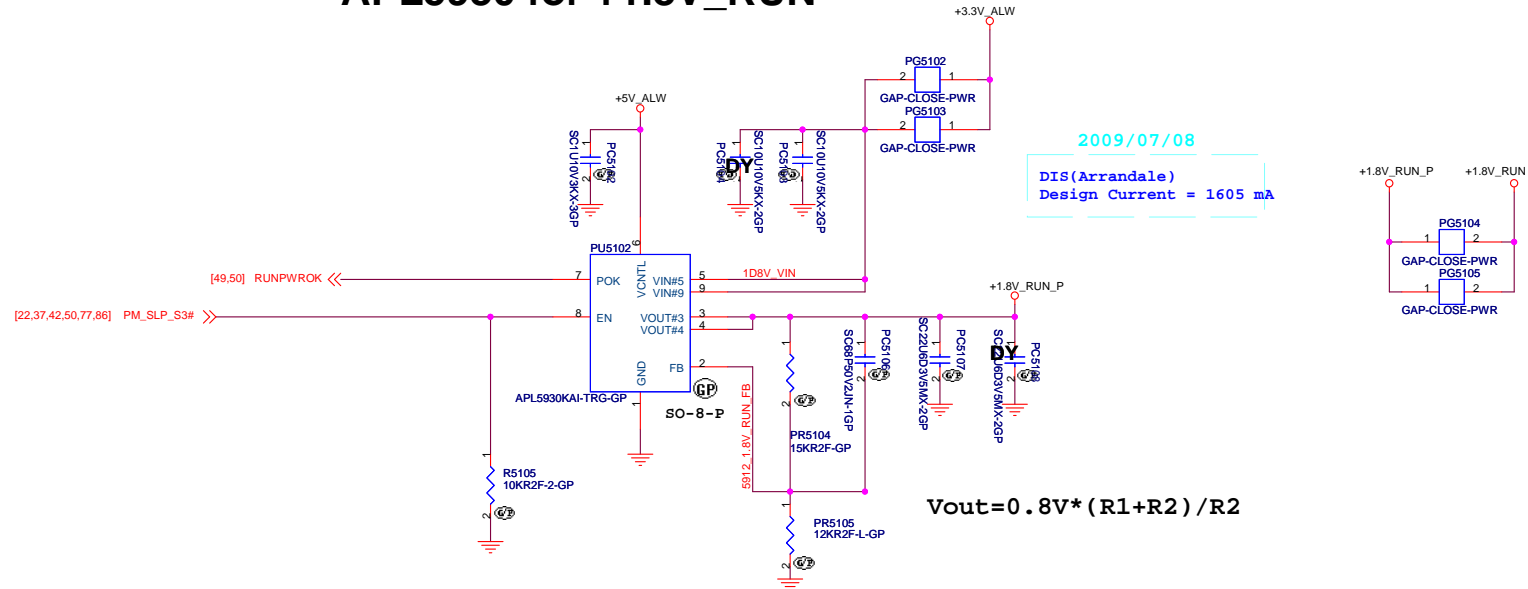
DELL **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Tito
TPS51116 +1.5V SUS

Size	Document Number	Rev
Custom	DW Calpella	X0
Date:	Monday, January 18, 2010	Sheet 50 of 91

SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN



www.aitech1.ru

<Core Design>

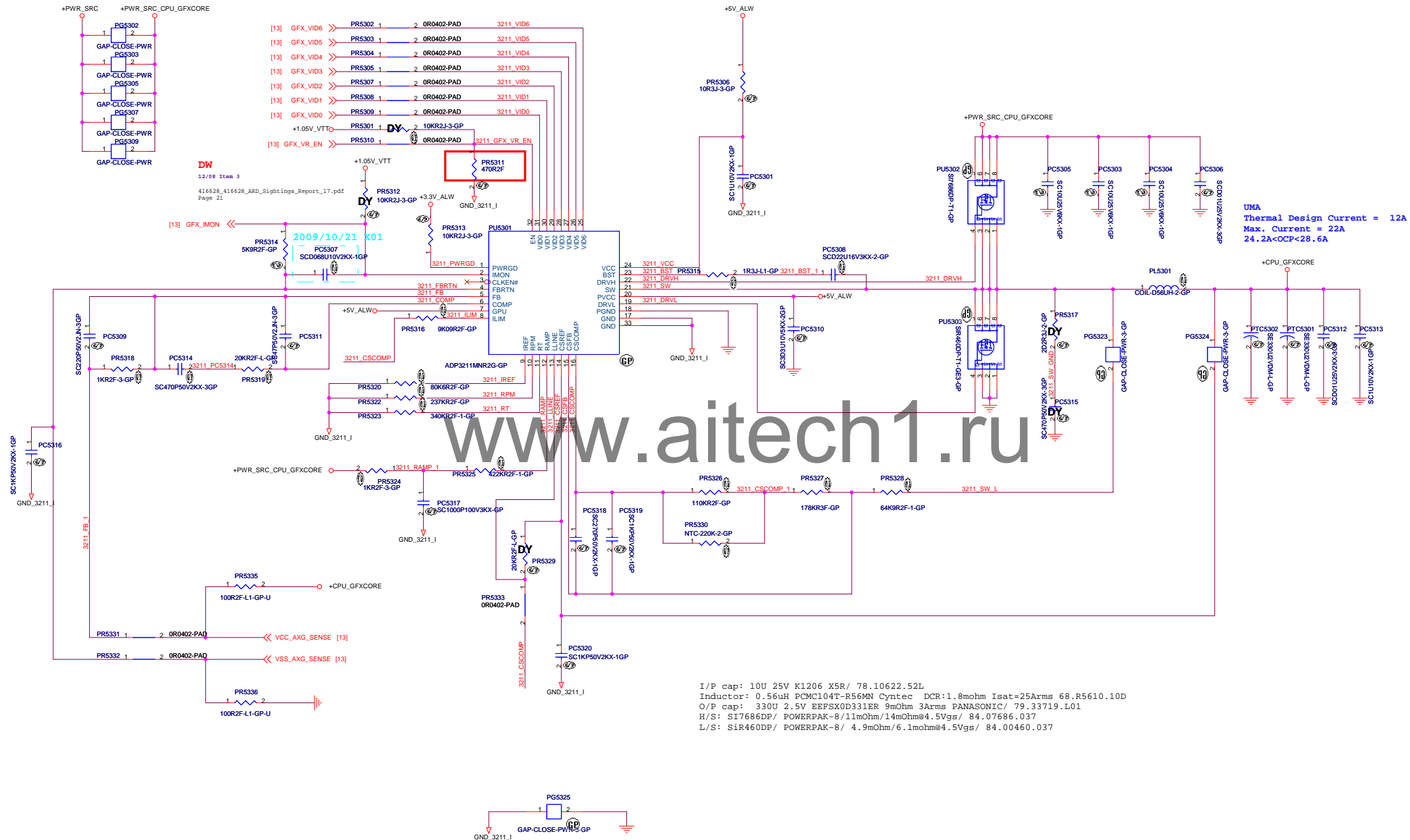


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title				
APL5930 +1.8V RUN				
Size	Document Number			Rev
Custom	DW Calpella			X01
Date: Monday, January 18, 2010		Sheet 51	of	91

(Blank)
www.aitech1.ru

SSID = CPU.GFX.Regulator



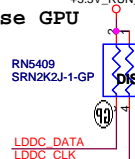
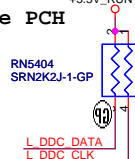
<Core Design>

DELL Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.	
Title ADP3211 CPU GFXCORE	
Size Customer	Document Number DW Calpella UMA
Date: Monday, January 18 2010	Rev X01
Sheet 53	of 91

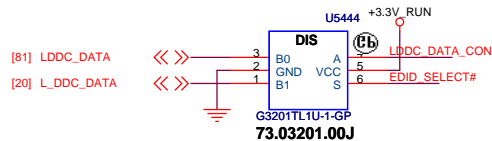
SSID = VIDEO

Close PCH

Close GPU

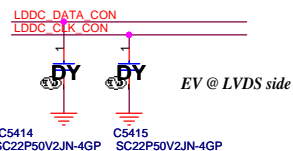
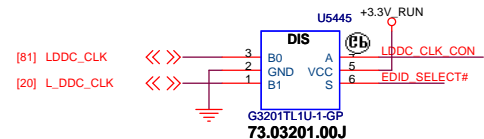


UMA/DIS LVDS DDC CLK/DAT select circuit



H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)

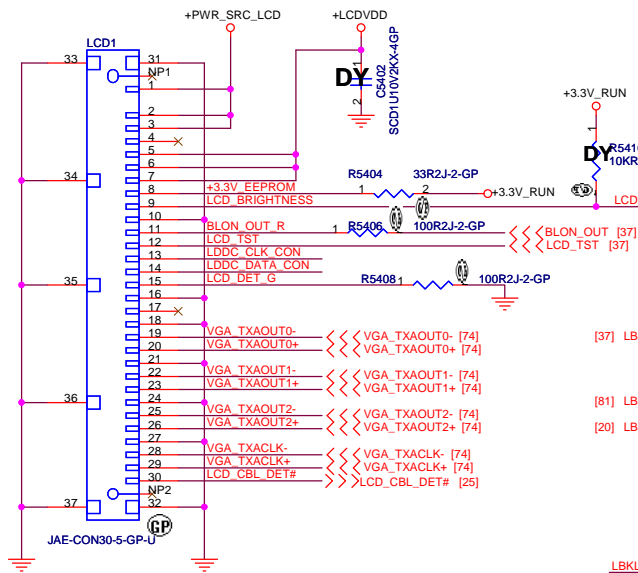
[21,55,57] EDID_SELECT# >>> EDID_SELECT#



EV @ LVDS side

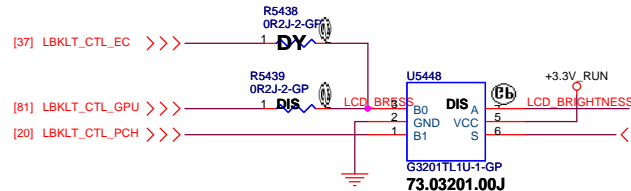
L DDC_DATA R5421 1 UMA 0R2J-2-GP LDDC_DATA_CON
L DDC_CLK R5420 1 UMA 0R2J-2-GP LDDC_CLK_CON

LVDS CONNECTOR



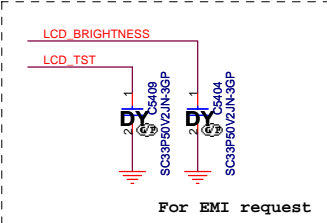
20.F1555.030

UMA/DIS LVDS PWM select circuit

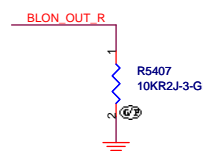


H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)

LBKLT_CTL_PCH R5422 1 UMA 0R2J-2-GP LCD_BRIGHTNESS
LBKLT_CTL_EC R5424 1 DY 0R2J-2-GP LCD_BRIGHTNESS

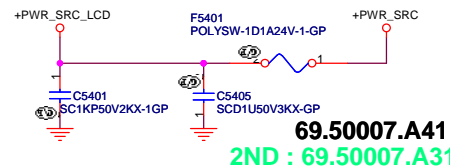


For EMI request



SSID = Inverter

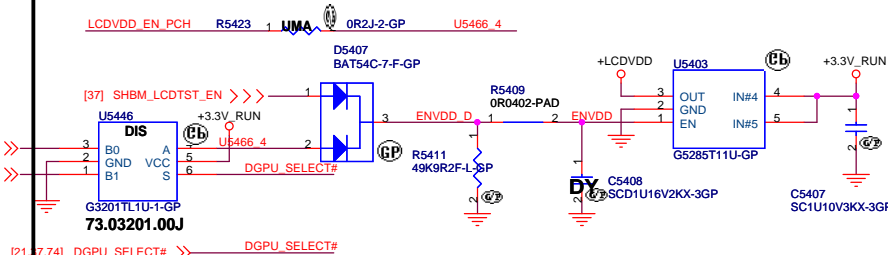
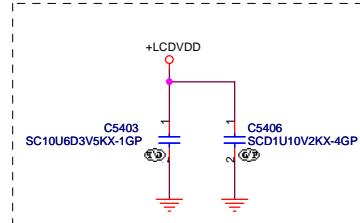
INVERTER POWER



69.50007.A41
2ND : 69.50007.A31

SSID = VIDEO

LCD POWER



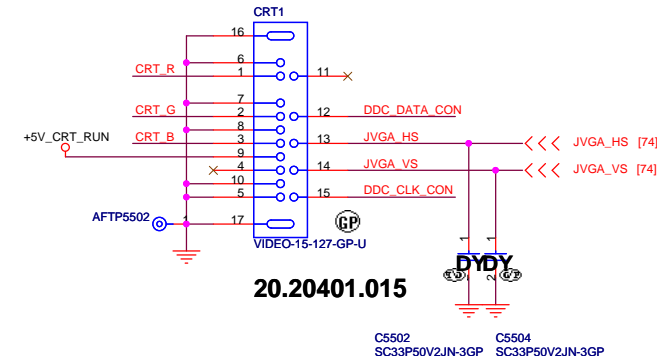
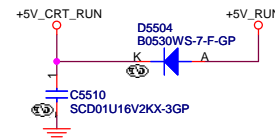
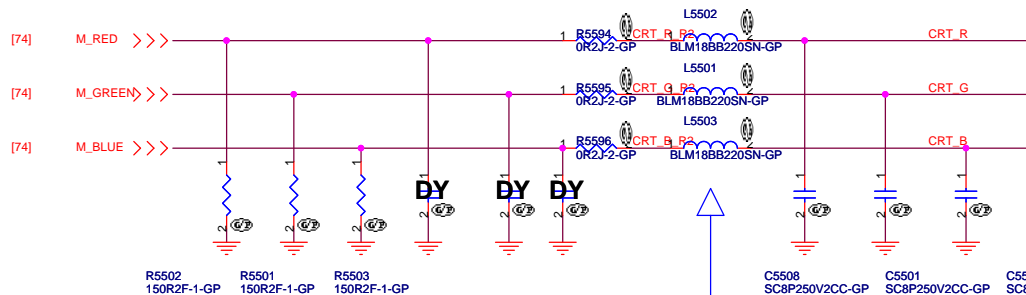
H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)

<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD/Inverter Connector		
Size	Document Number	Rev	X01
Custom	Vostro Calpella		
Date: Monday, January 18, 2010	Sheet 54	of	91

SSID = VIDEO



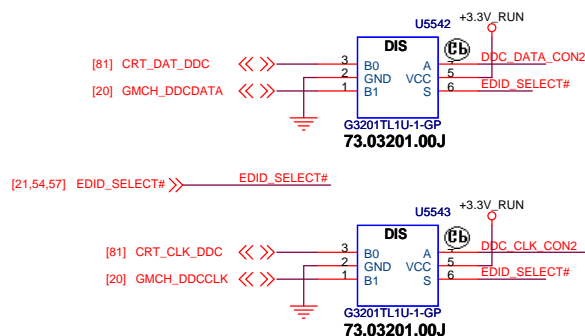
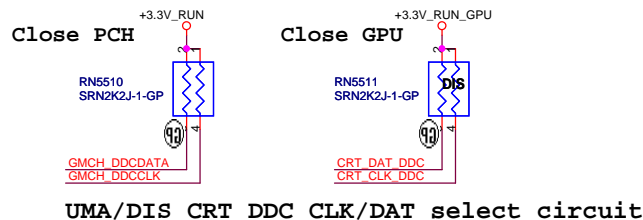
Layout Note:

*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.

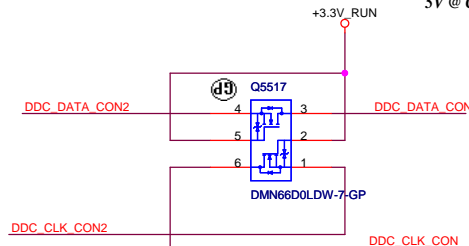
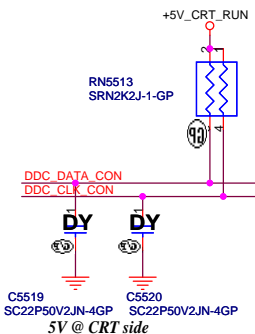
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.

- AFTP5503 1 +5V_CRT_RUN
- AFTP5501 1 DDC_DATA_CON
- AFTP5509 1 DDC_CLK_CON
- AFTP5507 1 CRT_R
- AFTP5506 1 CRT_G
- AFTP5508 1 CRT_B
- AFTP5504 1 JVGA_HS
- AFTP5505 1 JVGA_VS

www.aitech1.ru



H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)




<Core Design>

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CRT Connector			
Size	Document Number	Rev	
A3	Vostro Calpella	X01	
Date: Monday, January 18, 2010	Sheet 55	of	91

(Blank)

www.aitech1.ru

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size

Document Number

Rev

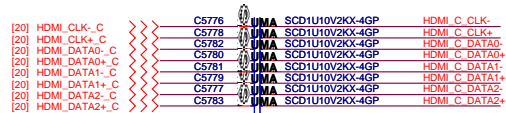
Custom

Vostro Calpella

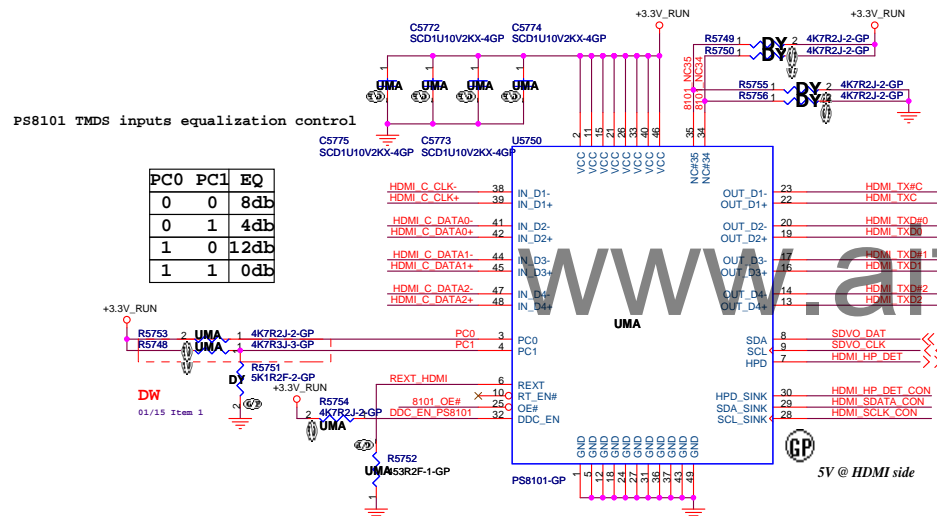
X01

Date: Monday, January 18, 2010Sheet 56 of 91

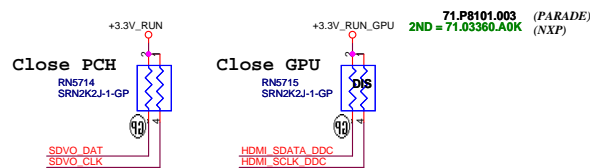
[81]	IFPC_D2+	>>>	C5769	DIS1	SCDU1U10V2KX-4GP	HDMI TXD2
[81]	IFPC_D2-	>>>	C5764	DIS1	SCDU1U10V2KX-4GP	HDMI TXD#2
[81]	IFPC_D1+	>>>	C5770	DIS1	SCDU1U10V2KX-4GP	HDMI TXD1
[81]	IFPC_D1-	>>>	C5765	DIS1	SCDU1U10V2KX-4GP	HDMI TXD#1
[81]	IFPC_D0+	>>>	C5768	DIS1	SCDU1U10V2KX-4GP	HDMI TXD0
[81]	IFPC_D0-	>>>	C5767	DIS1	SCDU1U10V2KX-4GP	HDMI TXD#0
[81]	IFPC_TXC+	>>>	C5771	DIS1	SCDU1U10V2KX-4GP	HDMI TXC
[81]	IFPC_TXC-	>>>	C5766	DIS1	SCDU1U10V2KX-4GP	HDMI TX#C



UMA HDMI level shift circuit



PC0	PC1	EQ
0	0	8db
0	1	4db
1	0	12db
1	1	0db



UMA/DIS HDMI DDC OR2J-2-GP

[B1] HDMI_SDATA_DDC << 3

[20] SDVO_DAT << 1

+3.3V RUN

HDMI_SDATA_CON L

EDID_SELECT#

DIS

BO GND VCC A

B1 S S

G3201TL1U-1-GP

73.03201.00J

OR2J-2-GP

1 2 3 4 5 6

1.2V

75747

[B1] HDMI_SCLK_DDC << 3

[20] SDVO_CLK << 1

+3.3V RUN

HDMI_SCLK_CON L

EDID_SELECT#

DIS

BO GND VCC A

B1 S S

G3201TL1U-1-GP

73.03201.00J

OR2J-2-GP

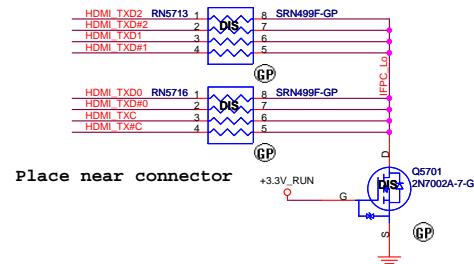
1 2 3 4 5 6

1.2V

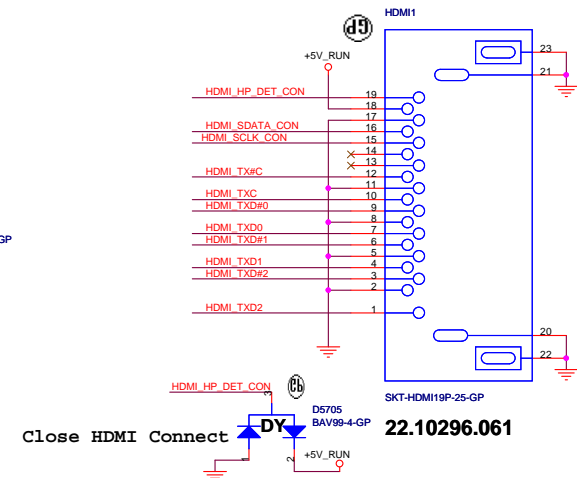
75747

H=>B1 -iGPU PCH (UMA)

L=>B0 -dGPU GPU (DIS)



Place near connector



[B1] HDMI_HP_DET_VGA <<< [20,21] HDMI_HP_DET <<<

R5745
15K
R5746
100K

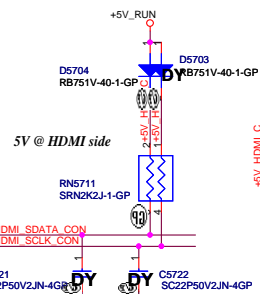
Close GPU

Close PCH

U5740 DIS
B0 B1
G3201TLIU-1-GP
73.03201.00J
EDID_SELECT# [21,54,55]

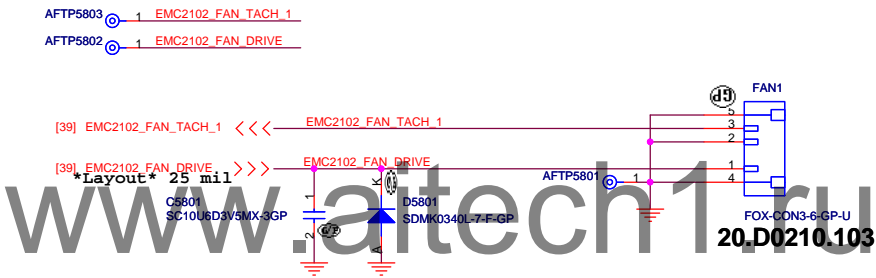
+3.3V_RUN
HDMI_HP_DET_3D3_CON <<<

H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)



SSID = Thermal

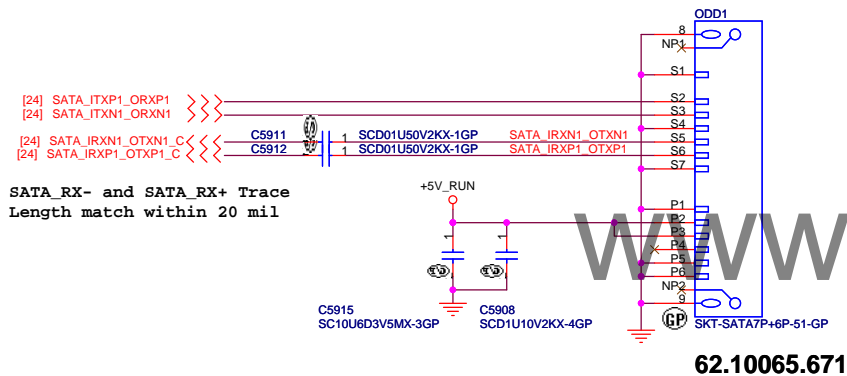
Fan Connector



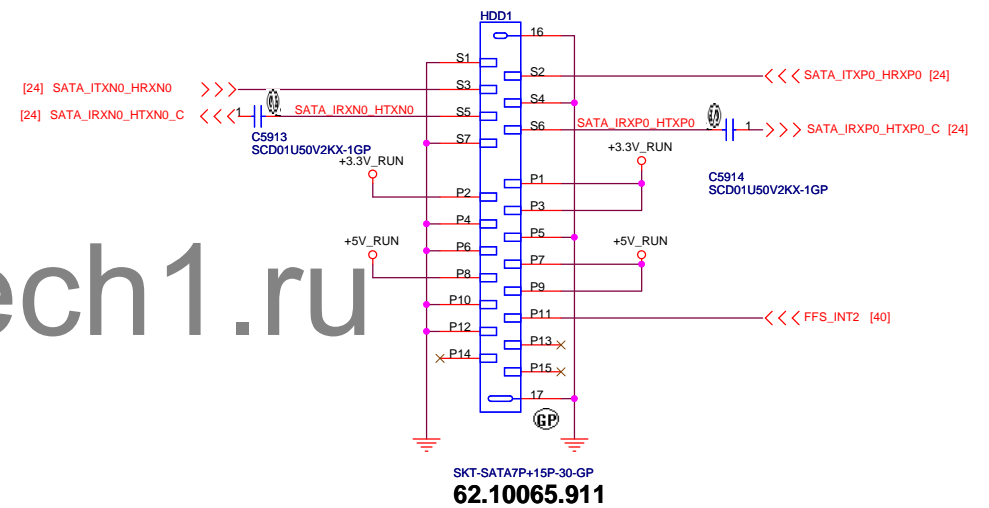
SSID = SATA

SSID = SATA

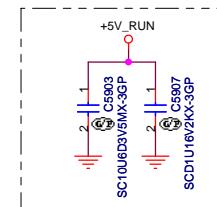
ODD Connector



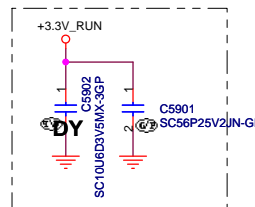
SATA HDD Connector



Close to CONN
5V power pin



Close to CONN
3.3V power pin



<Core Design>




Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			Rev
HDD/ODD Connector			X01
Size A3	Document Number Vostro Calpella		
Date: Monday, January 18, 2010	Sheet 59	of	91

(Blank)

www.aitech1.ru

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)


Size	Document Number	Rev
Custom	Vostro Calpella	X01

Date: Monday, January 18, 2010Sheet 60 of 91

(Blank)

www.aitech1.ru

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

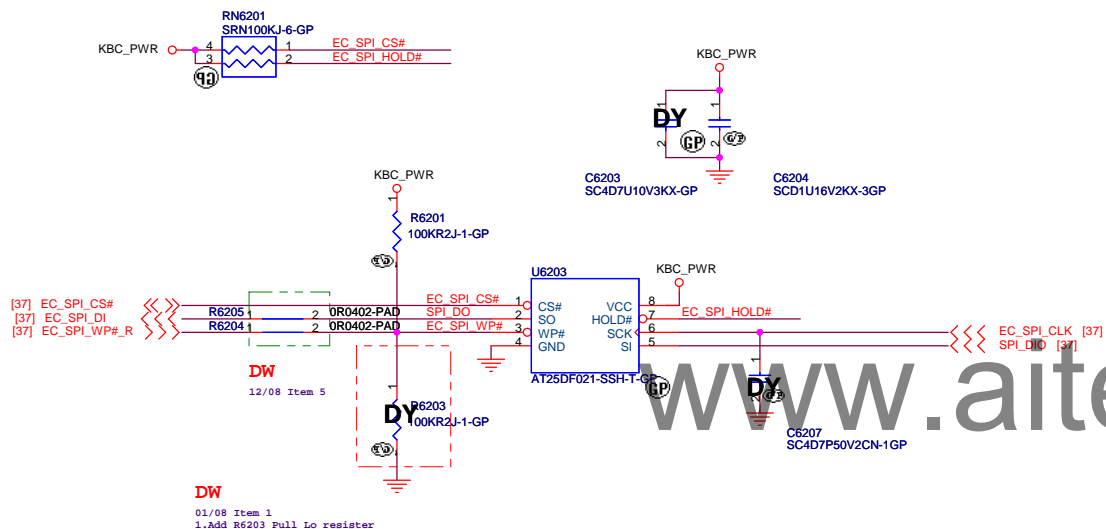
(Reserve)

Size	Document Number	Rev
Custom	Vostro Calpella	X01

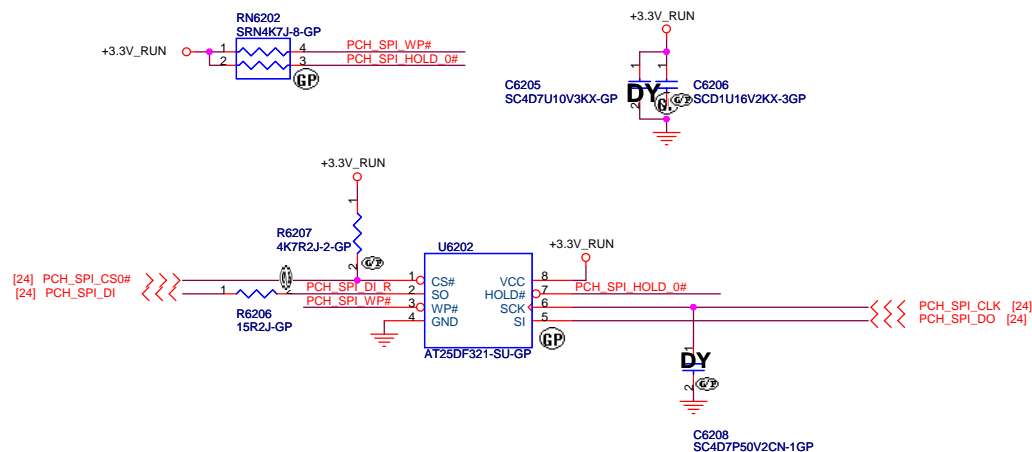
Date: Monday, January 18, 2010	Sheet 61 of 91
--------------------------------	----------------

```
SSID = Flash.ROM
```

SPI FLASH ROM (256K bytes) for KBC

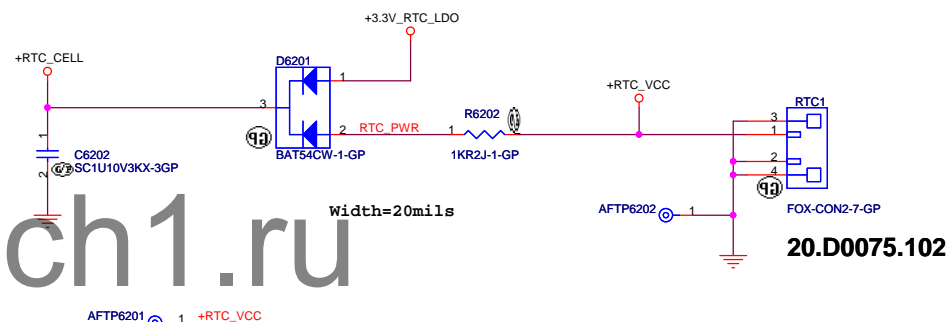


SPI FLASH ROM (4M bytes) for PCH



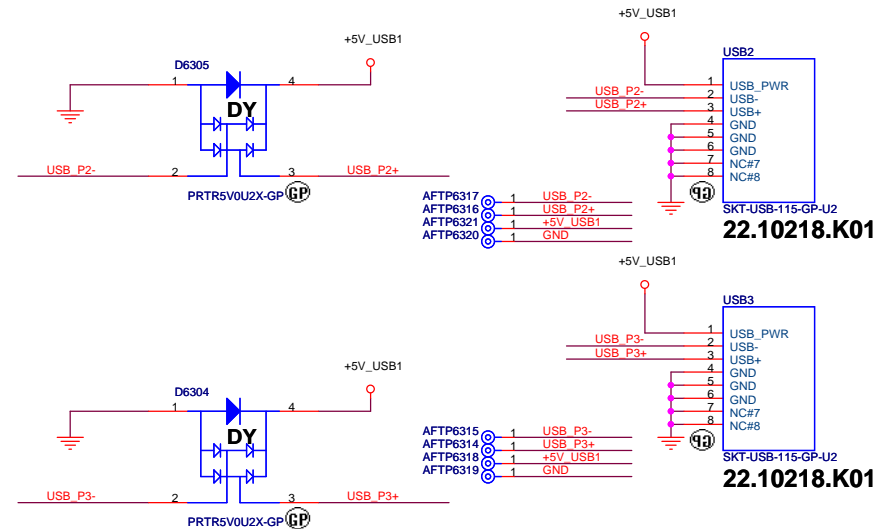
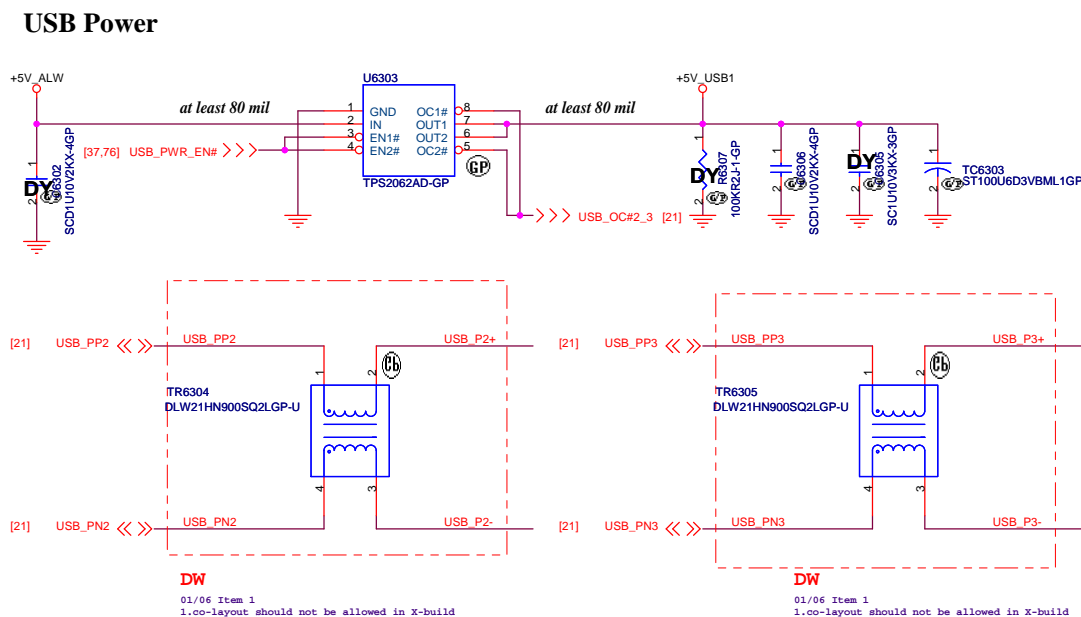
SSID = RBATT

RTC Connector

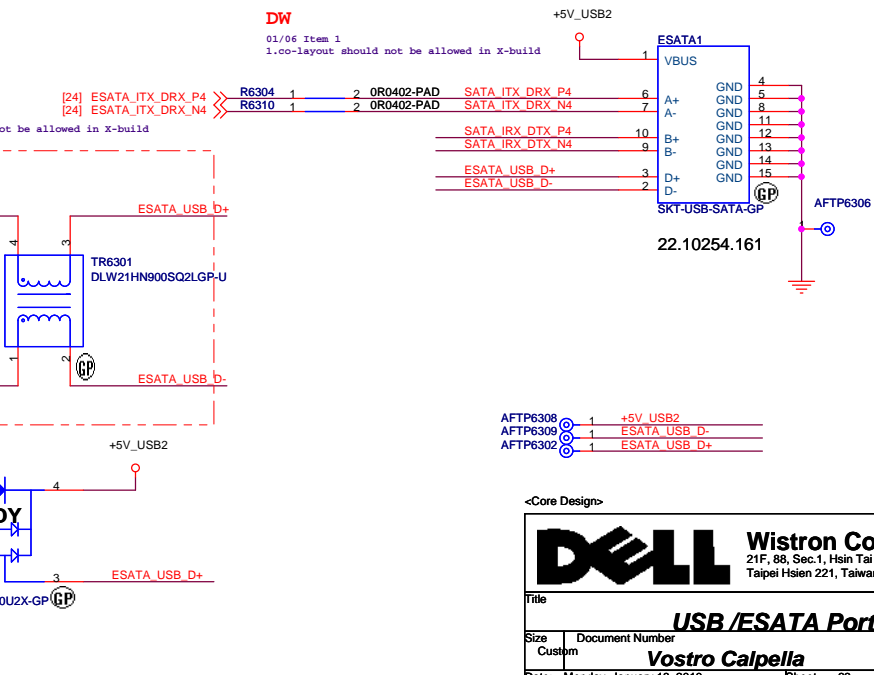
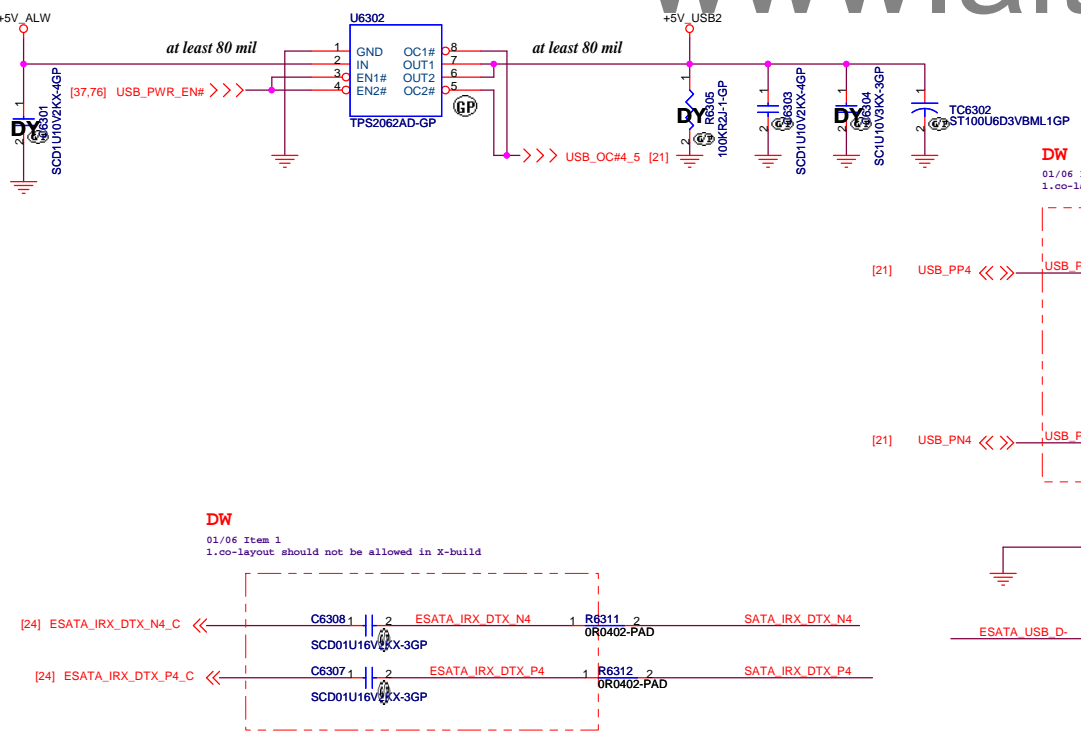


SSID = USB

USB Power

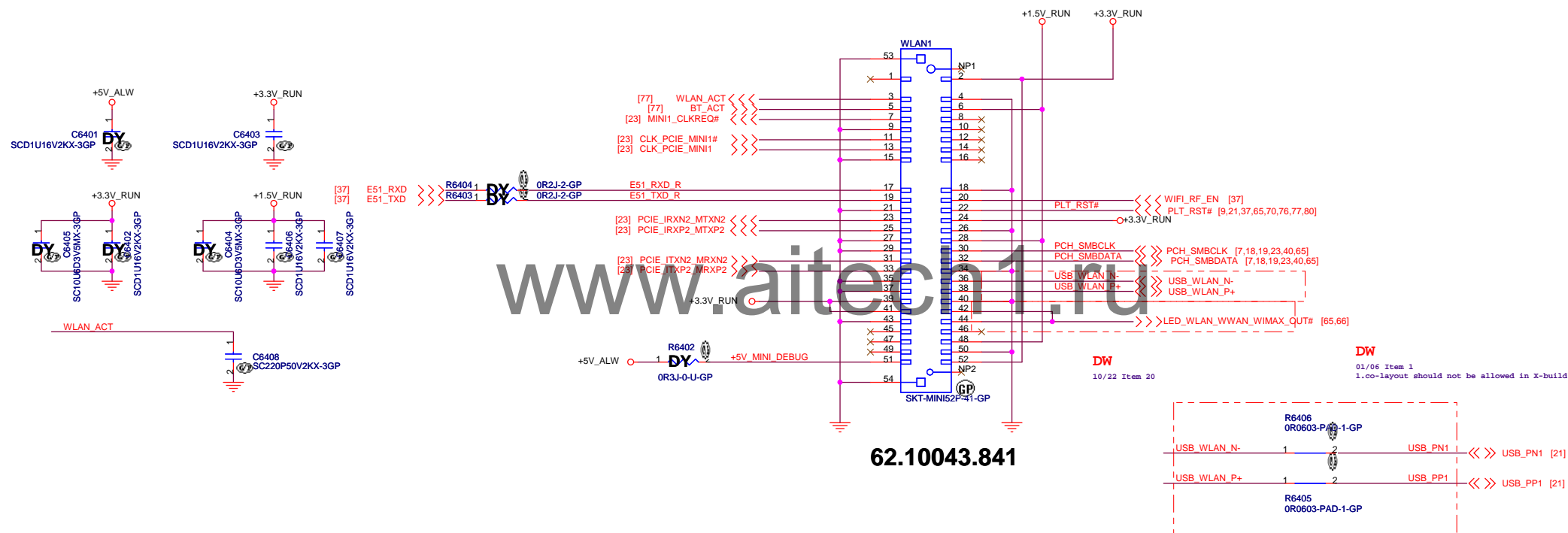


ESATA Power



SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

MINICARD(WLAN)/ITP CONN

Size

Document Number

Rev

A3

Vostro Calpella

X01

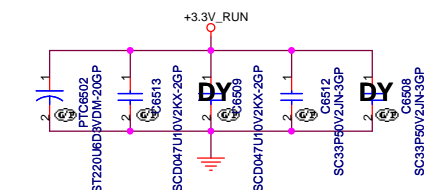
Date: Monday, January 18, 2010

Sheet 64 of 91

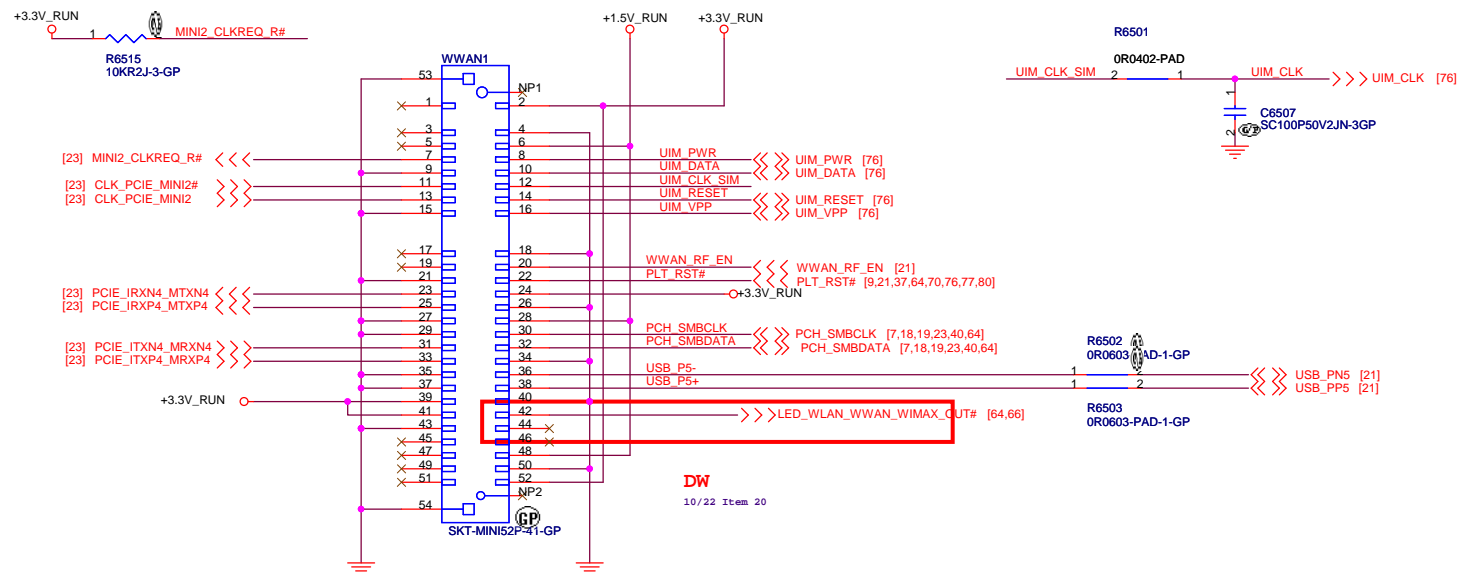
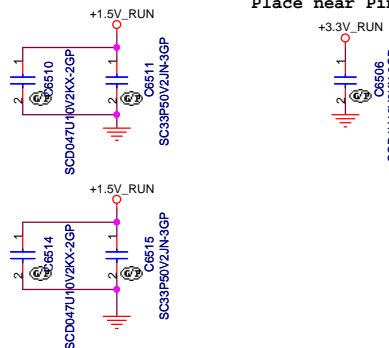
SSID = Wireless

Mini Card Connector(WWAN)

Place near MINI Card CONN



Place near Pin 24



www.aitech1.ru

<Core Design>



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

WWAN Connector

Size
A3

Document Number

Vostro Calpella

Rev

X01

Date: Monday, January 18, 2010

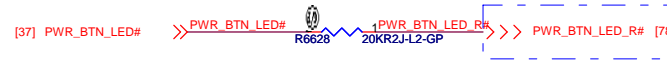
Sheet 65 of 91

For LED & Capacity board:

LED Type	Color	Power rail
SCRL LED	White	ALW
CAP LED	White	ALW
NUM LED	White	ALW
PWR BTN LED	White	ALW
SATA ACT LED1	White	RUN
BT ACT LED	White	RUN
WLAN WWAN WIMAX LED	White	RUN

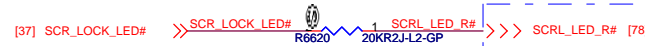
PWR BTN LED

For LED & Capacity board



SCRLK LED

For LED & Capacity board:



CAPS LED



NUM LED



Remove BJT to daughter board

Bluetooth LED

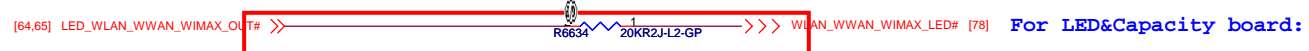
For LED & Capacity board:



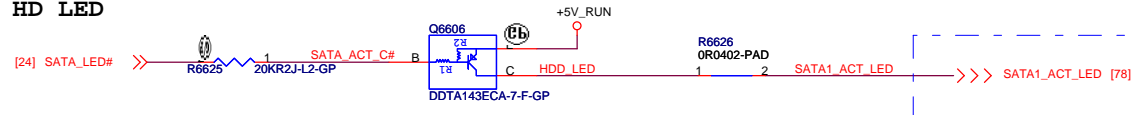
For IO board

LED Type	Color	Power rail
PWR LED2	White(Multi-color)	ALW
BATTERY LED2	Amber(Multi-color)	ALW
	White(Multi-color)	ALW

www.aitech1.ru
DW
10/22 Item 20
WLAN WWAN WIMAX LED



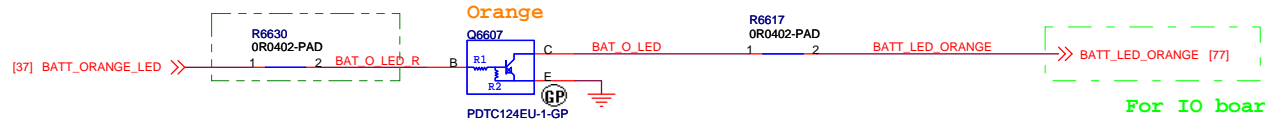
HD LED



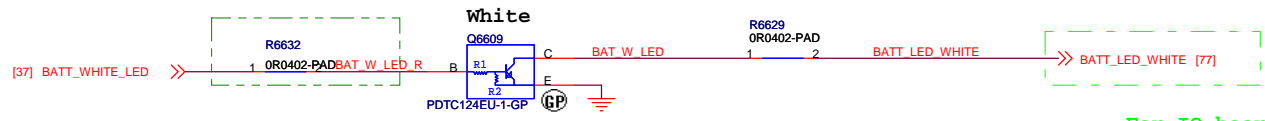
Battery & Power LED

DW

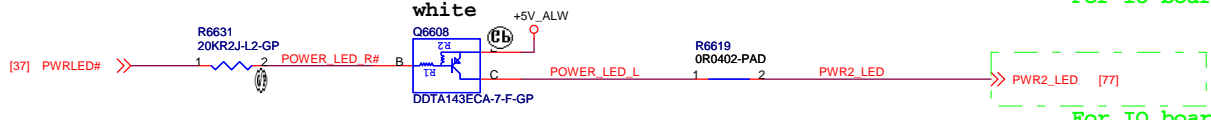
12/08 Item 5



For IO board



For IO board



For IO board

<Core Design>


DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
LED		
Size A3	Document Number Vostro Calpella	Rev X01
Date: Monday, January 18, 2010	Sheet 66 of 91	

(Blank)

www.aitech1.ru

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size
Custom

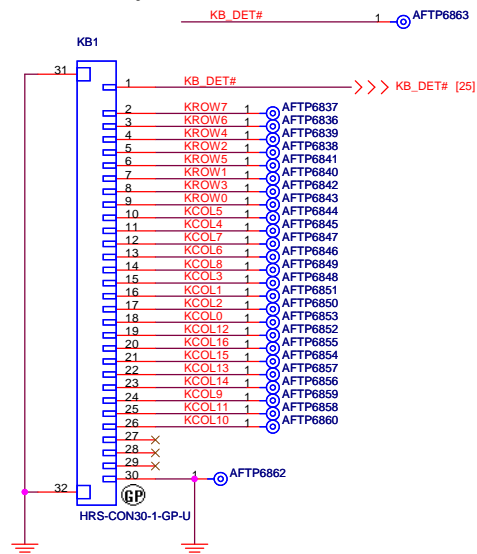
Document Number
Vostro Calpella

Rev
X01

Date: Monday, January 18, 2010Sheet 67 of 91

SSID = KBC

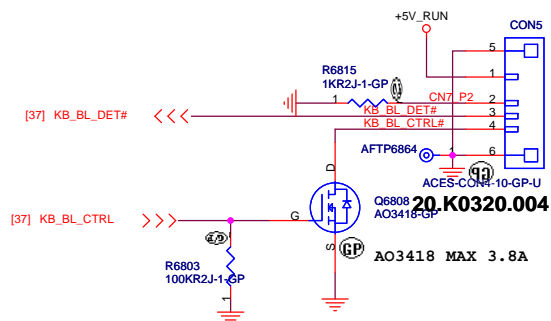
Internal Keyboard Connector



20.K0259.030

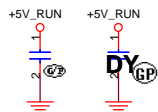
www.aitech1.ru

KB Backlight CONN



20.K0320.004

AFTP6833 1 +5V_RUN
AFTP6832 1 CN7 P2
AFTP6834 1 KB_BL_DET#
AFTP6861 1 KB_BL_CTRL#

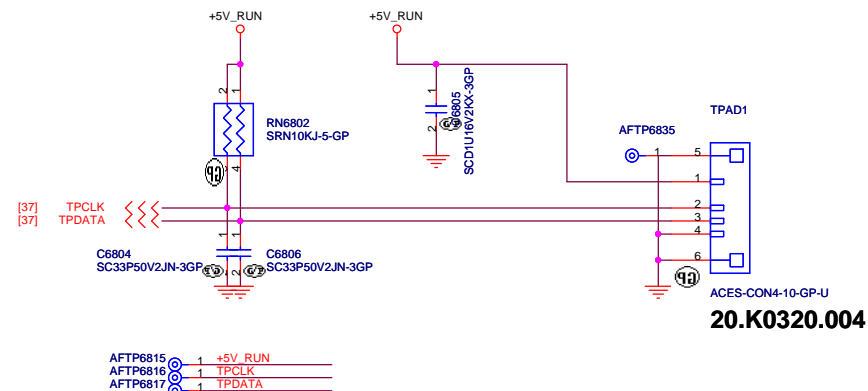


C6812 SCD1U25V2ZY-1GP C6895 SC4D7U10V5KX-1GP

Place near CON5

SSID = Touch.Pad

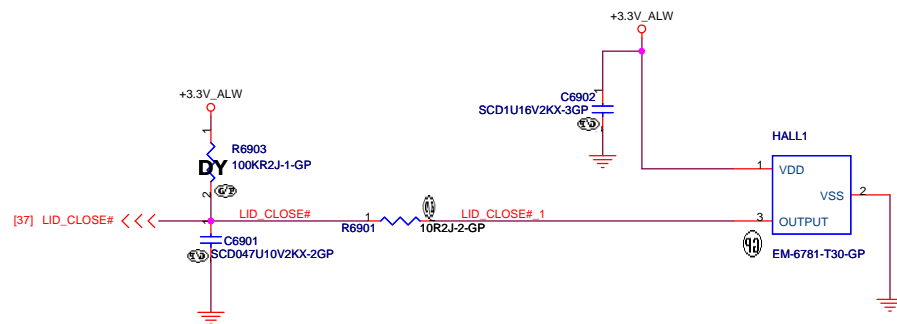
TouchPad Connector



<Core Design>

DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
Keyboard/Touch Pad			
Size	Document Number	Rev	
Custom	Vostro Calpella	X01	
Date:	Monday, January 18, 2010	Sheet	68 of 91

Hall Sensor Connector



www.aitech1.ru

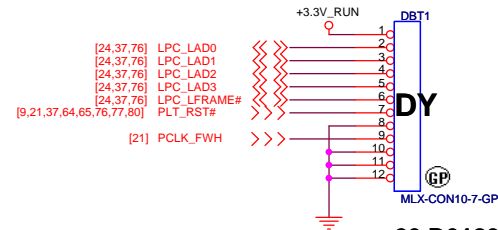
<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			Hall sensor	
Size	Document Number	Rev		
Custom	Vostro Calpella	X01		
Date:	Monday, January 18, 2010	Sheet	69	of 91

GOLDEN FINGER FOR DEBUG BOARD



20.D0183.110

www.aitech1.ru

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.


Title		
Debug port		
Size	Document Number	Rev
Custom	Vostro Calpella	X01
Date:	Monday, January 18, 2010	Sheet 70 of 91

www.aitech1.ru

(Blank)

www.aitech1.ru

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size

Document Number

Rev

Custom

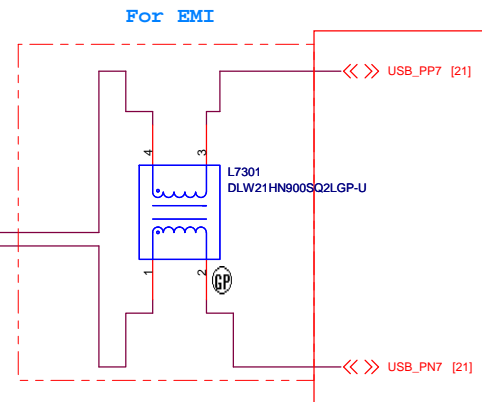
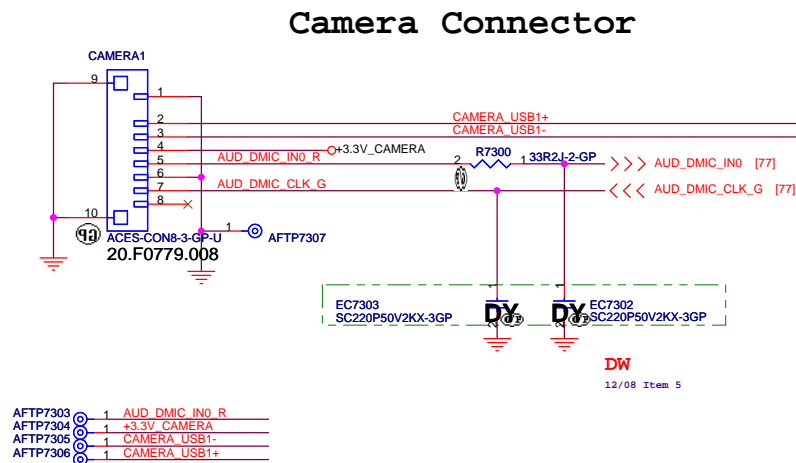
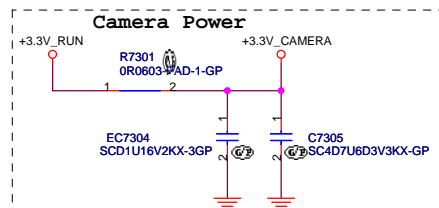
Vostro Calpella

X01

Date: Monday, January 18, 2010

Sheet 72 of 91

SSID = User.Interface



DW
01/18 Item 1

DW
01/06 Item 1
1.co-layout should not be allowed in X-build

DW
12/08 Item 5

AFTP7303 1 AUD_DMIC_IN0_R
AFTP7304 1 +3.3V_CAMERA
AFTP7305 1 CAMERA_USB1-
AFTP7306 1 CAMERA_USB1+

www.aitech1.ru

<Core Design>



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Camera CONN

Size

Document Number

Rev

A3

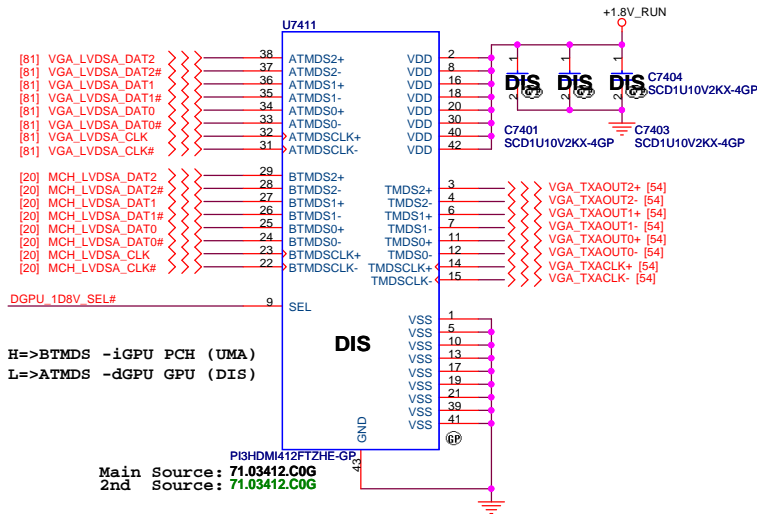
Vostro Montevina Discrete

X01

Date: Monday, January 18, 2010

Sheet 73 of 91

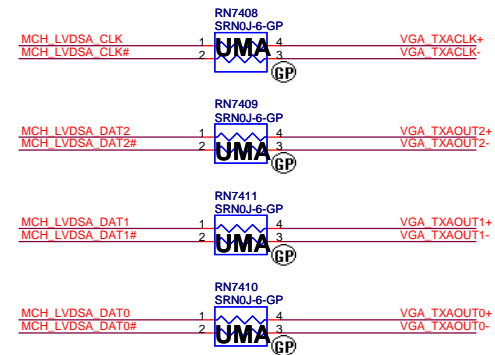
UMA/DIS LVDS signal select circuit



FUNCTION TABLE

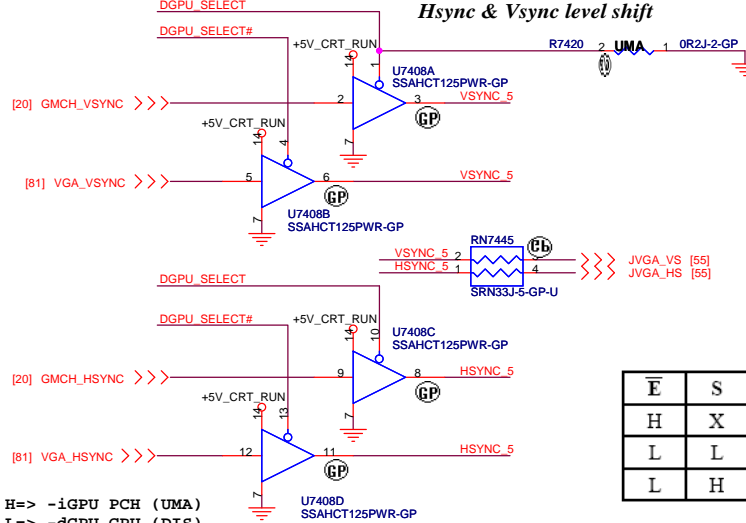
SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCCLK+ TMDSCLK- = ATMDSCCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCCLK+ = High Impedance ATMDSCCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

UMA LVDS signal circuit

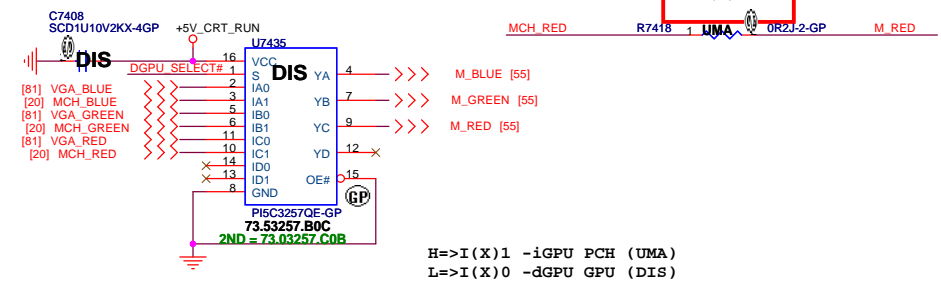


UMA/DIS CRT Hsync/Vsync select circuit

Hsync & Vsync level shift



UMA/DIS CRT signal select circuit



E	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

<Core Design>

DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: Swith-1			
Size: Custom	Document Number: Vostro Calpella	Rev: X01	
Date: Monday, January 18, 2010	Sheet: 74	of 91	

(Blank)

www.aitech1.ru

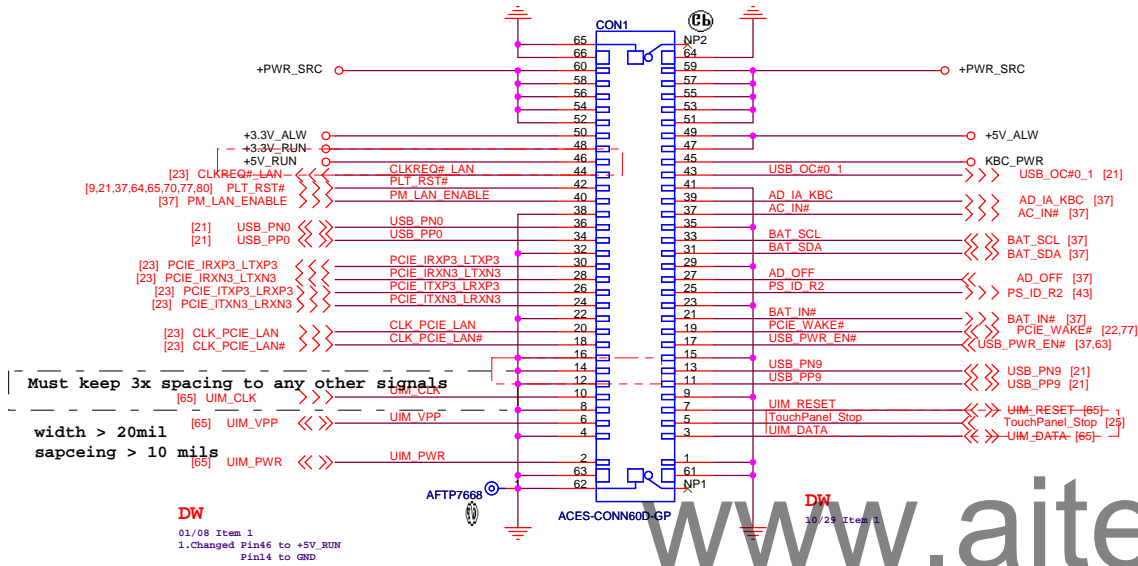
<Core Design>



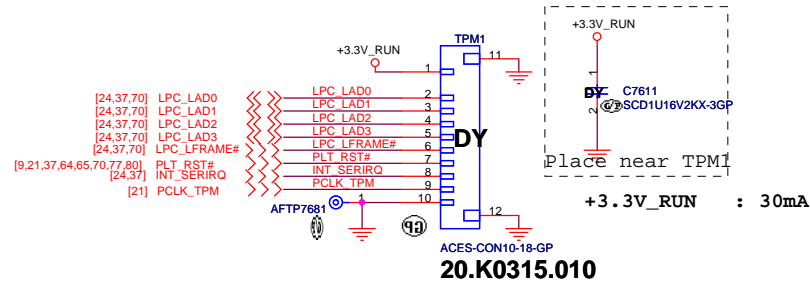
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			Reserve		
Size	Document Number				Rev
A3	Vostro Calpella				X01
Date: Monday, January 18, 2010		Sheet	75	of	91

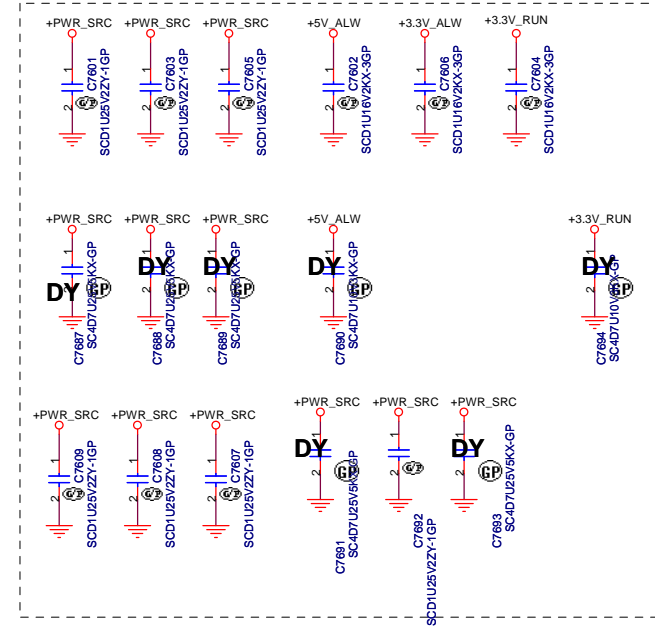
DC_IN board CON



TPM board CON



Place near CON1

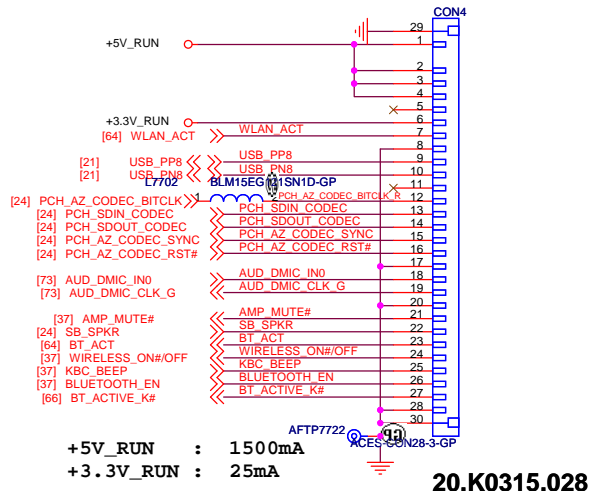


DW
01/08 Item 1
1.Remove DC-IN Board AFTP

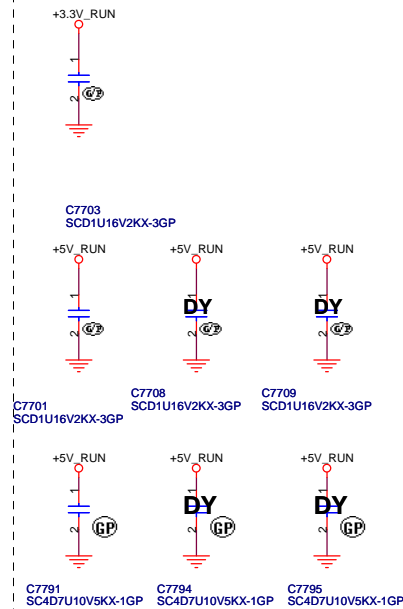
<Core Design>

SSID = User.Interface

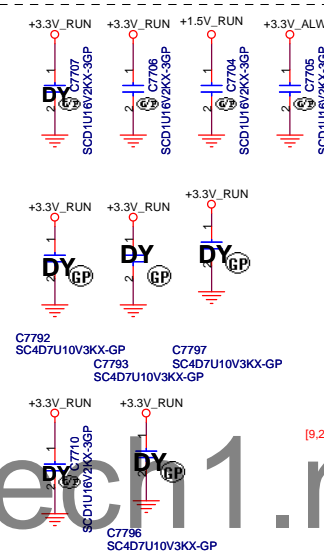
Audio board CON



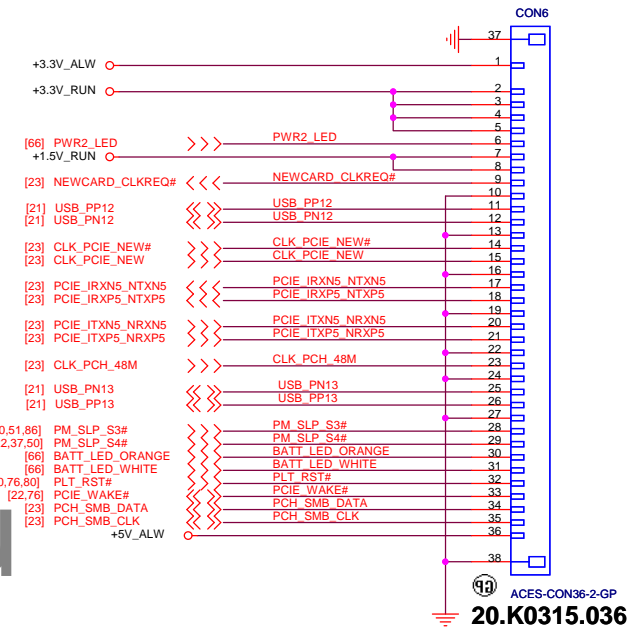
Place near CON4



Place near CON6



IO board CON

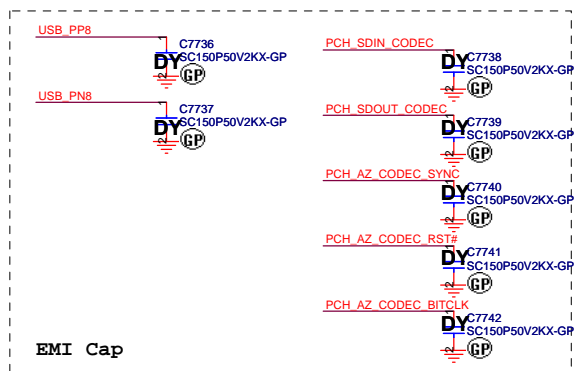


www.aitech1.ru

AFTP7710	1	+5V_RUN
AFTP7708	1	+3.3V_RUN
AFTP7709	1	WIRELESS_ON#OFF
AFTP7702	1	WLAN_ACT
AFTP7703	1	BLUETOOTH_EN
AFTP7704	1	BT_ACTIVE_K#
AFTP7705	1	BT_ACT
AFTP7707	1	USB_PP8
AFTP7708	1	USB_PN8
AFTP7712	1	PCH_AZ_CODEC_BITCLK_R
AFTP7713	1	PCH_SDIN_CODEC
AFTP7714	1	PCH_SDOUT_CODEC
AFTP7715	1	PCH_AZ_CODEC_SYNC
AFTP7716	1	PCH_AZ_CODEC_RST#
AFTP7718	1	SB_SPKR
AFTP7719	1	KBC_BEEP
AFTP7720	1	AUD_DMIC_IN0
AFTP7721	1	AUD_DMIC_CLK_G
AFTP7723	1	AMP_MUTE#

AFTP7758	1	+3.3V_ALW
AFTP7757	1	+3.3V_RUN
AFTP7760	1	+1.5V_RUN
AFTP7762	1	USB_PN12
AFTP7759	1	USB_PP12
AFTP7769	1	NEWCARD_CLKREQ#
AFTP7768	1	PCH_SMB_CLK
AFTP7767	1	PCH_SMB_DATA
AFTP7777	1	PM_SLP_S3#
AFTP7776	1	PM_SLP_S4#
AFTP7773	1	BATT_LED_ORANGE
AFTP7772	1	PWR2_LED
AFTP7781	1	PLT_RST#
AFTP7785	1	BATT_LED_WHITE
AFTP7787	1	+5V_ALW
AFTP7771	1	CLK_PCIE_NEW#
AFTP7770	1	CLK_PCIE_NEW
AFTP7761	1	PCIE_IRXN5_NTXN5
AFTP7765	1	PCIE_IRXP5_NTXP5
AFTP7764	1	PCIE_ITXN5_NRXN5
AFTP7763	1	PCIE_ITXP5_NRXN5
AFTP7775	1	USB_PN13
AFTP7766	1	USB_PP13
AFTP7774	1	PCIE_WAKE#
AFTP7778	1	CLK_PCH_48M

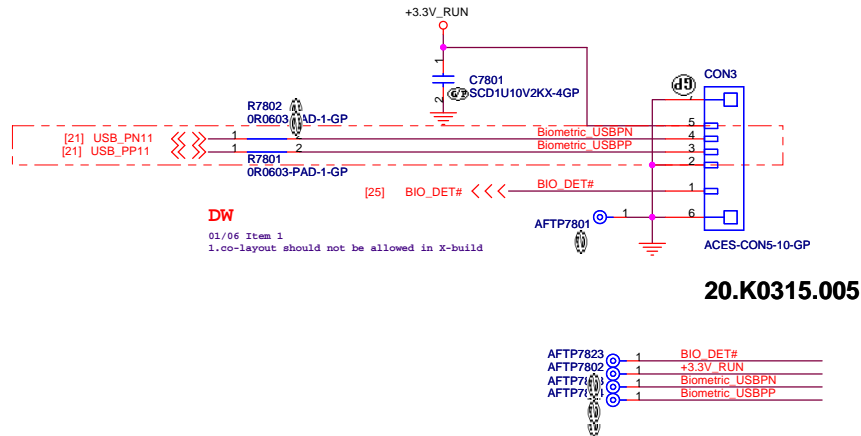
+1.5V_RUN : 650mA
+3.3V_RUN : 1775mA
+3.3V_ALW : 275mA
+5V_ALW: 60mA



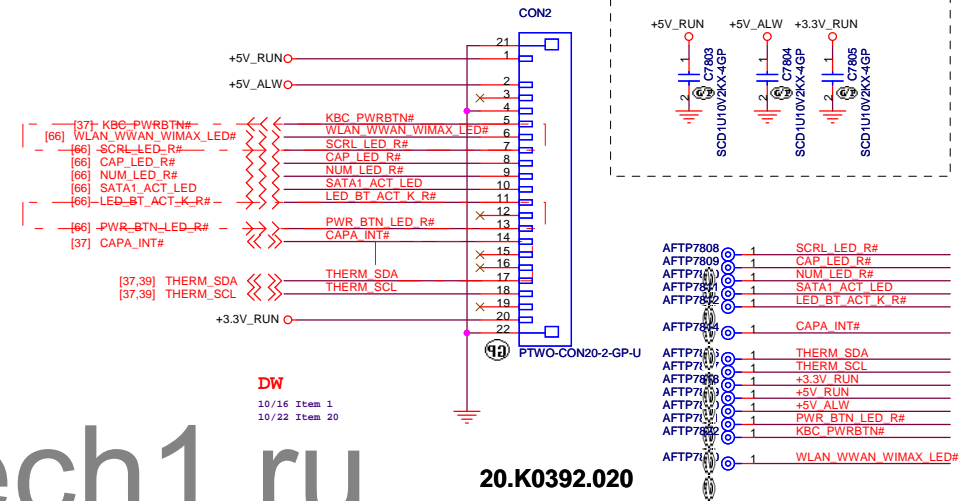
<Core Design>

DELL Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Audio BD/IO BD CONN		
Size Custom	Document Number Vostro Montevina Discrete	Rev X01
Date: Monday, January 18, 2010	Sheet 77 of 91	

Finger Printer Connector

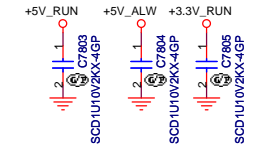


LED&Capacity board CONN



+3.3V_RUN : 3.5mA
+5V_RUN : 240mA
+5V_ALW : 80mA

Close to CON2



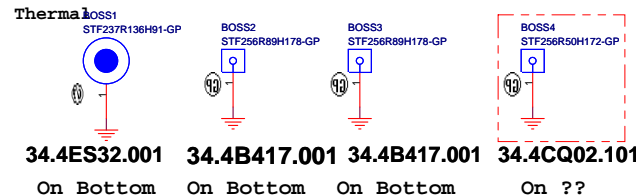
www.aitech1.ru

<Core Design>

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Finger Printer/Capacity			
Size	Document Number	Rev	
Custom	Vostro Calpella	X01	
Date: Monday, January 18, 2010	Sheet 78	of	91

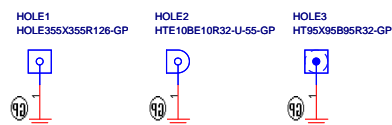
SSID = Mechanical

BOSS:

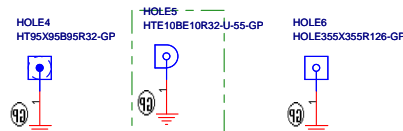


HOLE:

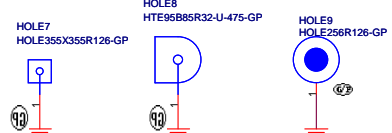
34.4ES31.001 34.4ES31.001



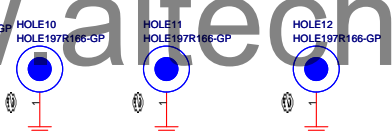
ZZ.00PAD.I71 ZZ.00PAD.K81 ZZ.00PAD.N81



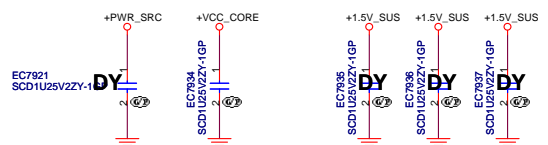
ZZ.00PAD.N81 **ZZ.00PAD.K81** ZZ.00PAD.I71



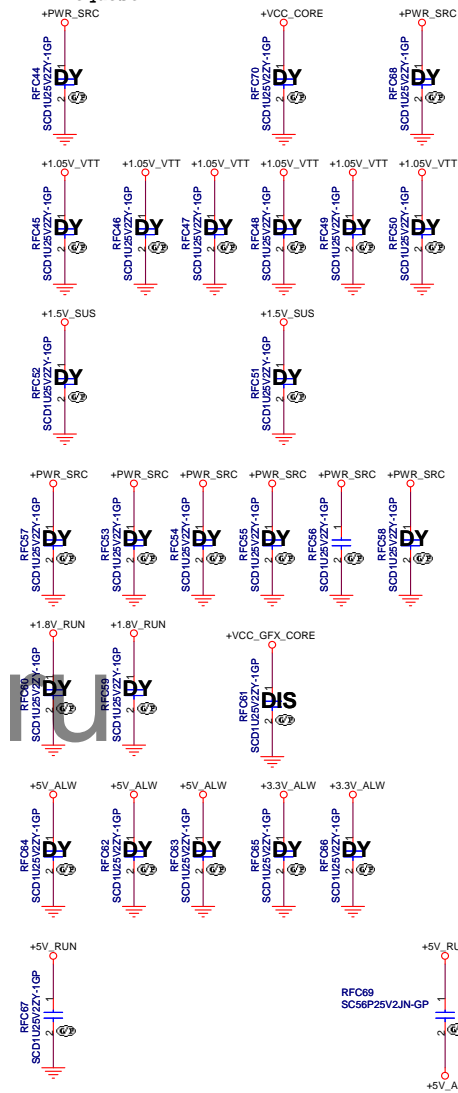
ZZ.00PAD.I71 ZZ.00PAD.N91 ZZ.00PAD.J01



34.4EM01.001 34.4EM01.001 34.4EM01.001



EMI Request



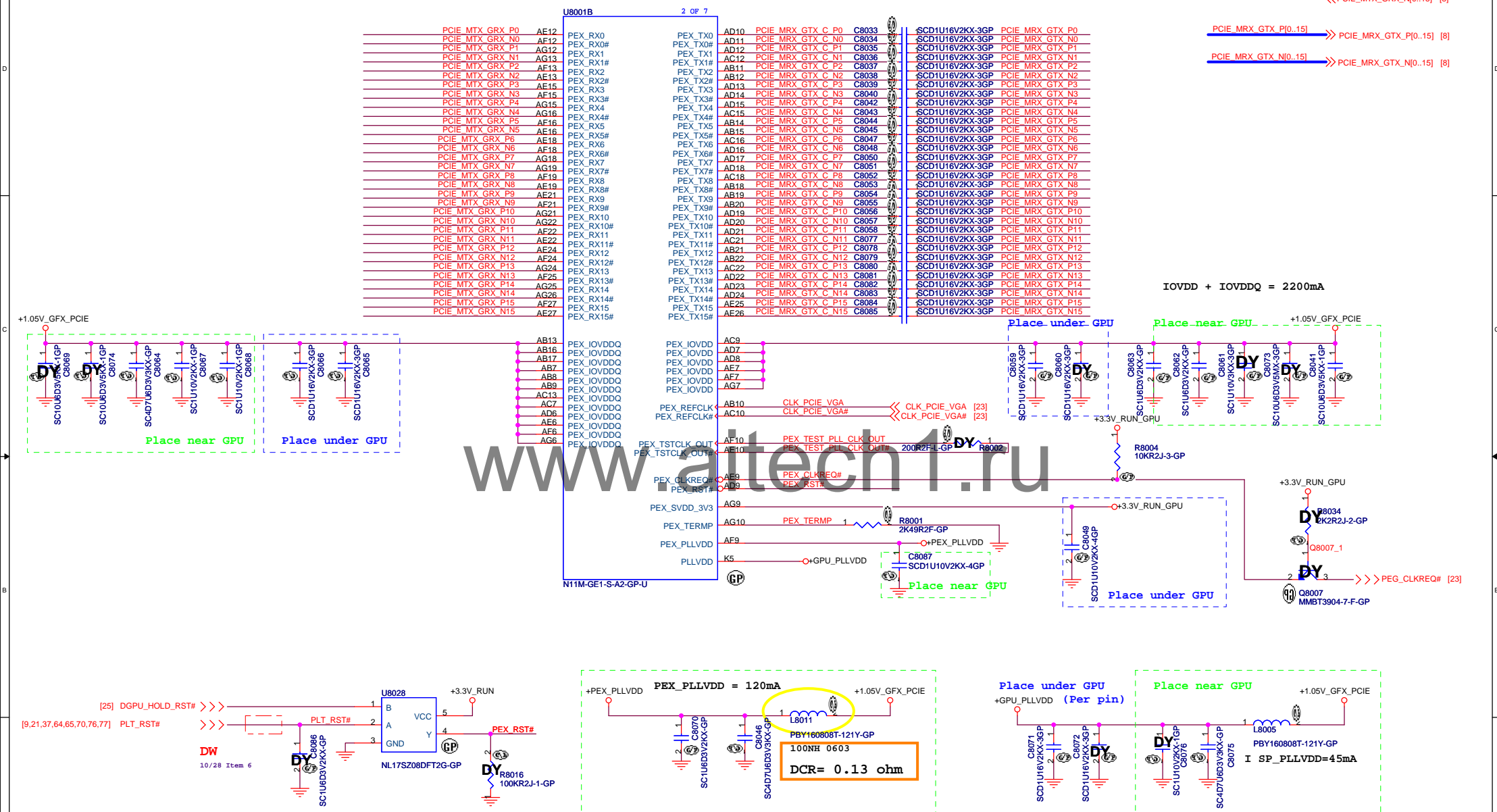
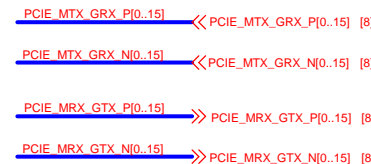
<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
Miscellaneous Components			
Size	Document Number	Rev	
Custom	Vostro Calpella	X	
Date: Monday, January 18, 2010		Sheet 79 of	91

SSID = VIDEO



<Core Design>

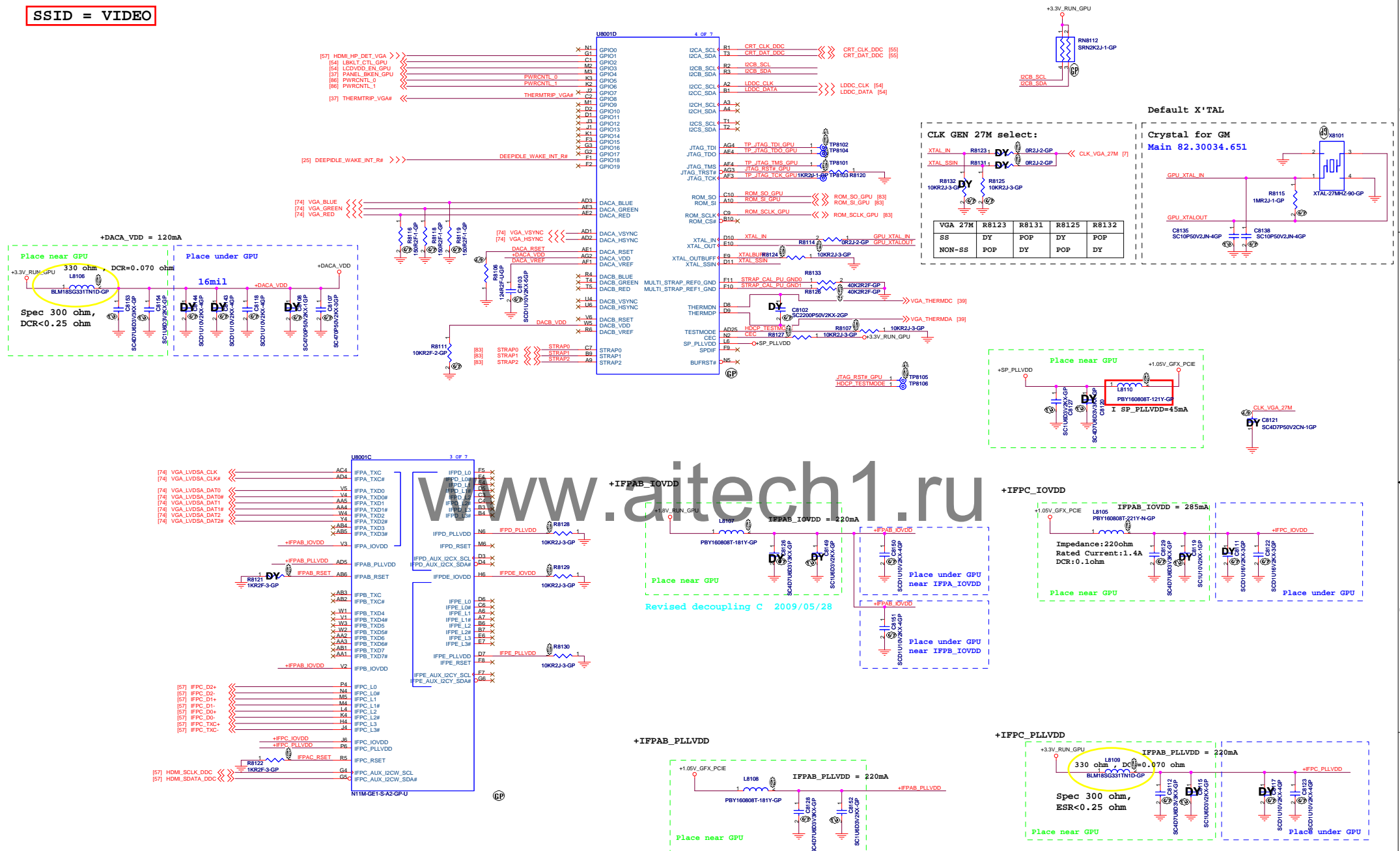


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

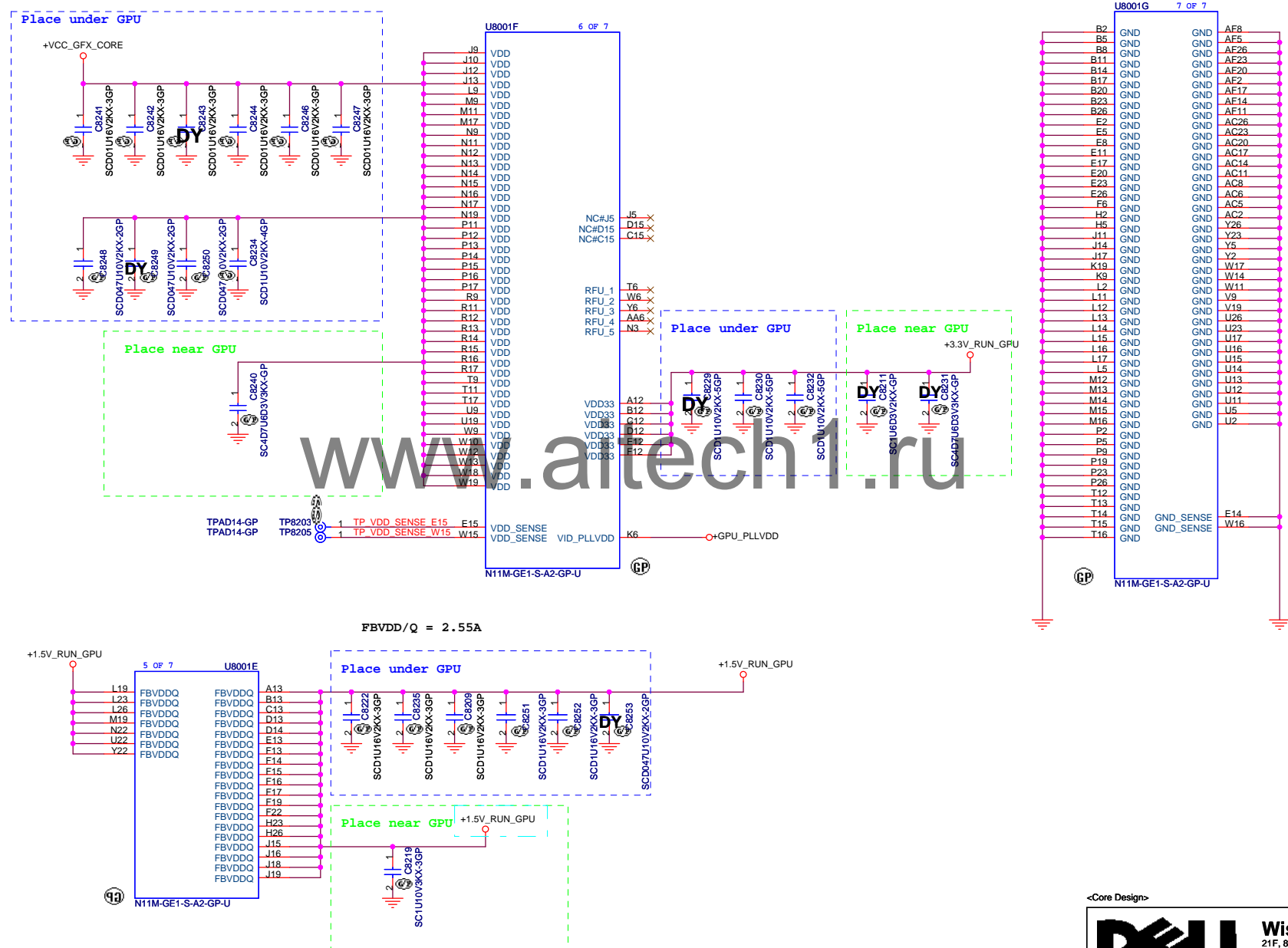
Title	VGA-PCIE/LVDS(1/4)
-------	---------------------------

Size A3	Document Number Vostro Calpella	Rev X01
Date: Monday, January 18, 2010	Sheet 80 of 91	

SSID = VIDEO



SSID = VIDEO



<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

VGA-POWER/GND(3/4)

Size
A

Document Number	
-----------------	--

Vostro Calpella

Rev
X01

Date: Monday, January 18, 2010

Sheet 82

32 of 91

SSID = VIDEO

[84,85] MDA[0..63]

U8001A

1 OF 7

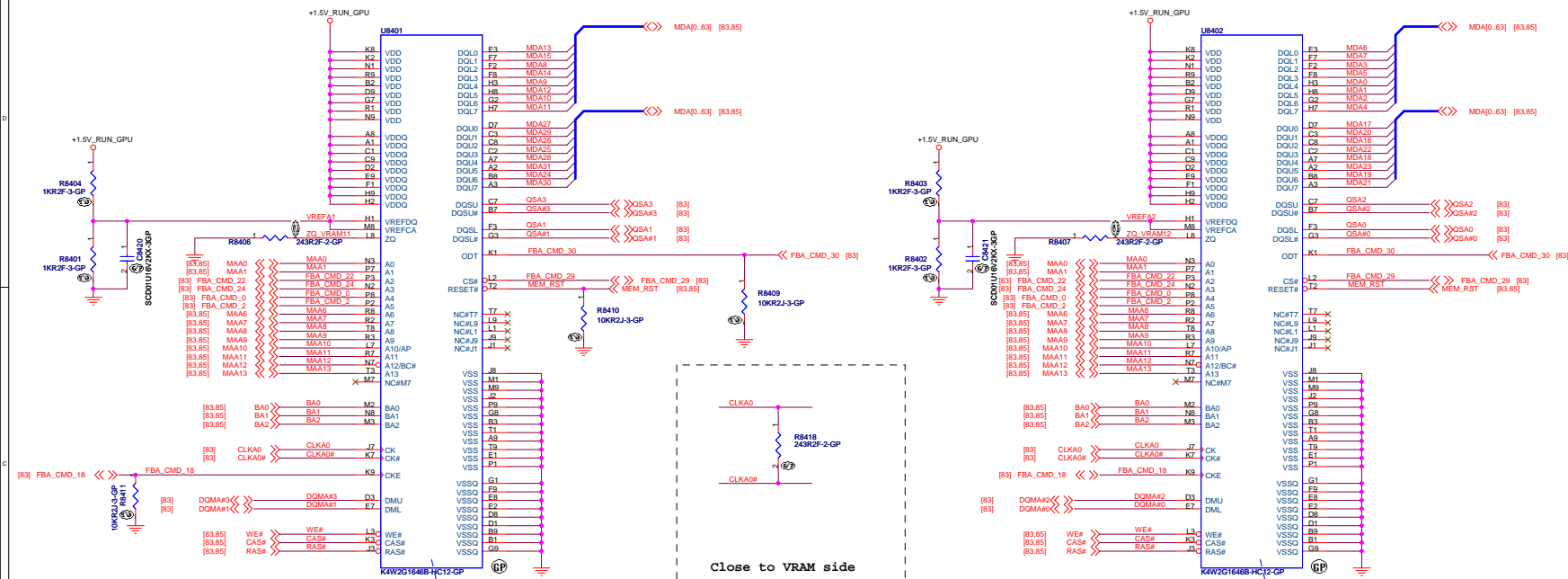
MDA0	D22	FBA_D0	FBA_CMD0	F26	FBA_CMD_0	<<>	FBA_CMD_0	[84]
MDA1	E24	FBA_D1	FBA_CMD1	J24	RAS#	<<>	RAS#	[84,85]
MDA2	E22	FBA_D2	FBA_CMD2	F26	FBA_CMD_2	<<>	FBA_CMD_2	[84]
MDA3	M24	FBA_D3	FBA_CMD3	M23	BA1	<<>	BA1	[84,85]
MDA4	D26	FBA_D4	FBA_CMD4	N27	FBA_CMD_4	<<>	FBA_CMD_4	[85]
MDA5	D27	FBA_D5	FBA_CMD5	M27	FBA_CMD_5	<<>	FBA_CMD_5	[85]
MDA6	C27	FBA_D6	FBA_CMD6	K26	FBA_CMD_6	<<>	FBA_CMD_6	[85]
MDA7	B27	FBA_D7	FBA_CMD7	J25	FBA_CMD_7	<<>	FBA_CMD_7	[85]
MDA8	A21	FBA_D8	FBA_CMD8	G23	FBA_CMD_8	<<>	FBA_CMD_8	[85]
MDA9	B21	FBA_D9	FBA_CMD9	G23	MAA11	<<>	MAA11	[84,85]
MDA10	C21	FBA_D10	FBA_CMD9	G26	CAS#	<<>	CAS#	[84,85]
MDA11	C19	FBA_D11	FBA_CMD10	J23	WE#	<<>	WE#	[84,85]
MDA12	C18	FBA_D12	FBA_CMD11	M25	BA0	<<>	BA0	[84,85]
MDA13	D18	FBA_D13	FBA_CMD12	K27	FBA_CMD_13	<<>	FBA_CMD_13	[85]
MDA14	B18	FBA_D14	FBA_CMD13	G25	MAA12	<<>	MAA12	[84,85]
MDA15	C16	FBA_D15	FBA_CMD14	L24	MEM_RST	<<>	MEM_RST	[84,85]
MDA16	F21	FBA_D16	FBA_CMD15	K24	MAA7	<<>	MAA7	[84,85]
MDA17	E21	FBA_D17	FBA_CMD16	K25	MAA0	<<>	MAA0	[84,85]
MDA18	D20	FBA_D18	FBA_CMD17	H22	MAA9	<<>	MAA9	[84,85]
MDA19	F20	FBA_D19	FBA_CMD18	L24	MAA8	<<>	MAA8	[84,85]
MDA20	D17	FBA_D20	FBA_CMD19	M26	FBA_CMD_22	<<>	FBA_CMD_22	[84]
MDA21	F18	FBA_D21	FBA_CMD20	F27	MAA8	<<>	MAA8	[84,85]
MDA22	E16	FBA_D22	FBA_CMD21	J26	FBA_CMD_24	<<>	FBA_CMD_24	[84]
MDA23	A22	FBA_D23	FBA_CMD22	G24	MAA1	<<>	MAA1	[84,85]
MDA24	C24	FBA_D24	FBA_CMD23	G27	MAA13	<<>	MAA13	[84,85]
MDA25	D21	FBA_D25	FBA_CMD24	M24	BA2	<<>	BA2	[84,85]
MDA26	B22	FBA_D26	FBA_CMD25	K22	FBA_CMD_28	<<>	FBA_CMD_28	[85]
MDA27	G22	FBA_D27	FBA_CMD26	J22	FBA_CMD_29	<<>	FBA_CMD_29	[84]
MDA28	A25	FBA_D28	FBA_CMD27	L22	FBA_CMD_30	<<>	FBA_CMD_30	[84]
MDA29	B25	FBA_D29	FBA_CMD28					
MDA30	A26	FBA_D30	FBA_CMD29					
MDA31	U24	FBA_D31	FBA_CMD30					
MDA32	V24	FBA_D32						
MDA33	V23	FBA_D33						
MDA34	T23	FBA_D34						
MDA35	R23	FBA_D35						
MDA36	P24	FBA_D36						
MDA37	P22	FBA_D37						
MDA38	AC24	FBA_D38						
MDA39	AB23	FBA_D39						
MDA40	W24	FBA_D40						
MDA41	W23	FBA_D41						
MDA42	W22	FBA_D42						
MDA43	W22	FBA_D43						
MDA44	W22	FBA_D44						
MDA45	W22	FBA_D45						
MDA46	W22	FBA_D46						
MDA47	W22	FBA_D47						
MDA48	W22	FBA_D48						
MDA49	W22	FBA_D49						
MDA50	W26	FBA_D50						
MDA51	W25	FBA_D51						
MDA52	AB25	FBA_D52						
MDA53	AB26	FBA_D53						
MDA54	AD26	FBA_D54						
MDA55	AD27	FBA_D55						
MDA56	V25	FBA_D56						
MDA57	R25	FBA_D57						
MDA58	V26	FBA_D58						
MDA59	V27	FBA_D59						
MDA60	R26	FBA_D60						
MDA61	T25	FBA_D61						
MDA62	N25	FBA_D62						
MDA63	N26	FBA_D63						

FBA_CMD0	F26	FBA_CMD_0	<<>	FBA_CMD_0	[84]
FBA_CMD1	J24	RAS#	<<>	RAS#	[84,85]
FBA_CMD2	F26	FBA_CMD_2	<<>	FBA_CMD_2	[84]
FBA_CMD3	M23	BA1	<<>	BA1	[84,85]
FBA_CMD4	N27	FBA_CMD_4	<<>	FBA_CMD_4	[85]
FBA_CMD5	M27	FBA_CMD_5	<<>	FBA_CMD_5	[85]
FBA_CMD6	K26	FBA_CMD_6	<<>	FBA_CMD_6	[85]
FBA_CMD7	J25	FBA_CMD_7	<<>	FBA_CMD_7	[85]
FBA_CMD8	G23	FBA_CMD_8	<<>	FBA_CMD_8	[85]
FBA_CMD9	G23	MAA11	<<>	MAA11	[84,85]
FBA_CMD10	G26	CAS#	<<>	CAS#	[84,85]
FBA_CMD11	J23	WE#	<<>	WE#	[84,85]
FBA_CMD12	M25	BA0	<<>	BA0	[84,85]
FBA_CMD13	K27	FBA_CMD_13	<<>	FBA_CMD_13	[85]
FBA_CMD14	G25	MAA12	<<>	MAA12	[84,85]
FBA_CMD15	L24	MEM_RST	<<>	MEM_RST	[84,85]
FBA_CMD16	K24	MAA7	<<>	MAA7	[84,85]
FBA_CMD17	K25	MAA0	<<>	MAA0	[84,85]
FBA_CMD18	H22	MAA9	<<>	MAA9	[84,85]
FBA_CMD19	L24	MAA8	<<>	MAA8	[84,85]
FBA_CMD20	M26	FBA_CMD_22	<<>	FBA_CMD_22	[84]
FBA_CMD21	F27	MAA8	<<>	MAA8	[84,85]
FBA_CMD22	J26	FBA_CMD_24	<<>	FBA_CMD_24	[84]
FBA_CMD23	G24	MAA1	<<>	MAA1	[84,85]
FBA_CMD24	G27	MAA13	<<>	MAA13	[84,85]
FBA_CMD25	M24	BA2	<<>	BA2	[84,85]
FBA_CMD26	K22	FBA_CMD_28	<<>	FBA_CMD_28	[85]
FBA_CMD27	J22	FBA_CMD_29	<<>	FBA_CMD_29	[84]
FBA_CMD28	L22	FBA_CMD_30	<<>	FBA_CMD_30	[84]

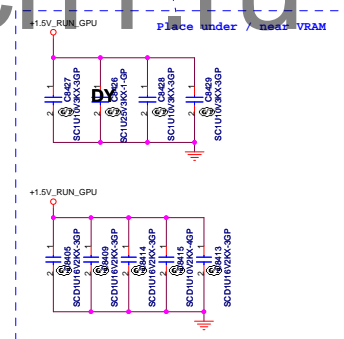
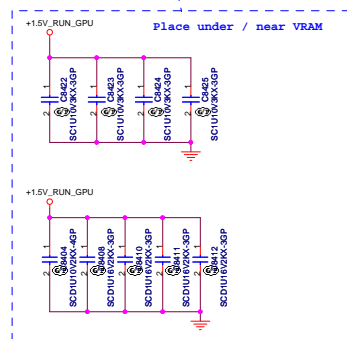
FBA_CMD29					
FBA_CMD30					
FBA_CMD31					
FBA_CMD32					
FBA_CMD33					
FBA_CMD34					
FBA_CMD35					
FBA_CMD36					
FBA_CMD37					
FBA_CMD38					
FBA_CMD39					
FBA_CMD40					
FBA_CMD41					
FBA_CMD42					
FBA_CMD43					
FBA_CMD44					
FBA_CMD45					
FBA_CMD46					
FBA_CMD47					
FBA_CMD48					
FBA_CMD49					
FBA_CMD50					
FBA_CMD51					
FBA_CMD52					
FBA_CMD53					
FBA_CMD54					
FBA_CMD55					
FBA_CMD56					
FBA_CMD57					
FBA_CMD58					
FBA_CMD59					
FBA_CMD60					
FBA_CMD61					
FBA_CMD62					
FBA_CMD63					

FBA_CMD0	C26	DQMA#0	DQMA#0	[8]
FBA_CMD1	B19	DQMA#1	DQMA#1	[8]
FBA_CMD2	D19	DQMA#2	DQMA#2	[8]
FBA_CMD3	D23	DQMA#3	DQMA#3	[8]
FBA_CMD4	T24	DQMA#4	DQMA#4	[8]
FBA_CMD5	AA23	DQMA#5	DQMA#5	[8]
FBA_CMD6	AB27	DQMA#6	DQMA#6	[8]
FBA_CMD7	T26	DQMA#7	DQMA#7	[8]

SS1D = VIDEO



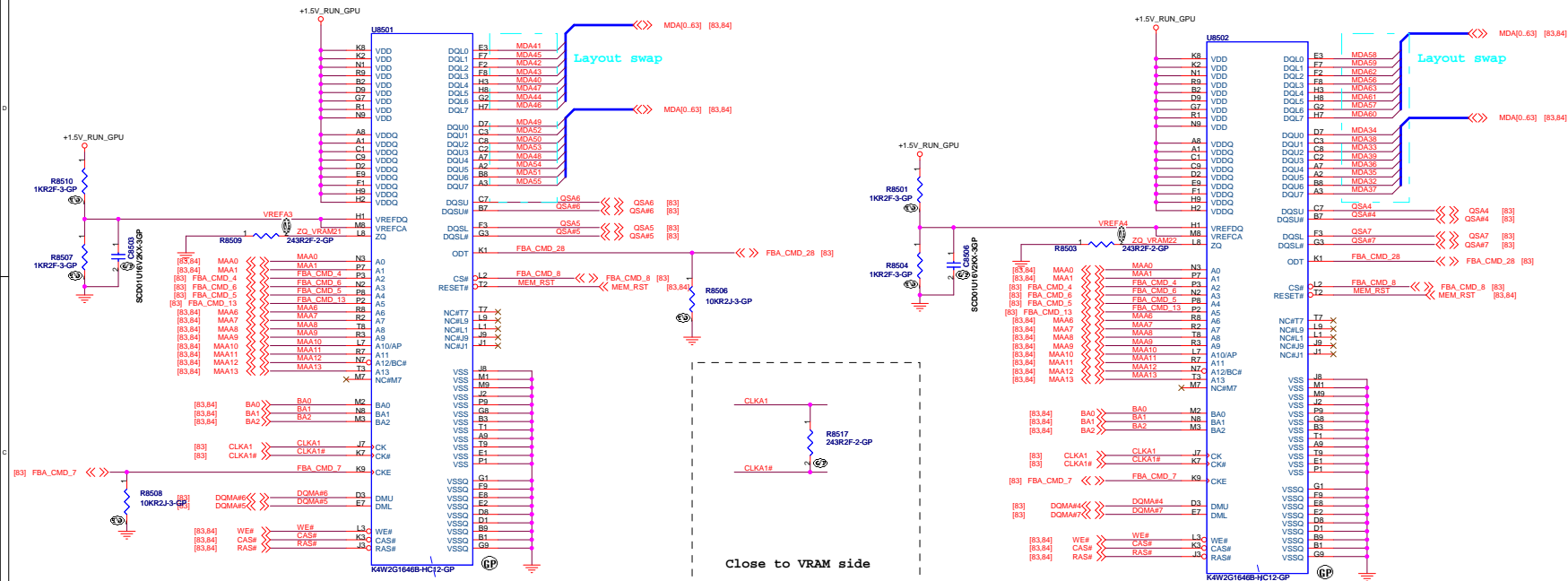
64X16 SAMSUNG K4W1G1646E-HC12 P/N:72.41164.H0U
64X16 HYNIX H5TQ1G63BFR-12C P/N:72.51G63.C0U



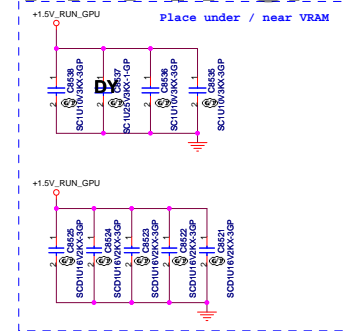
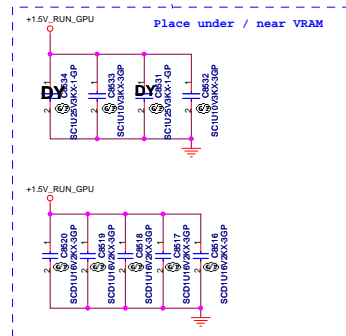
www.aitech1.ru

<Core Design>

SS1D = VIDEO



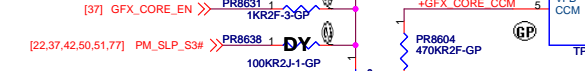
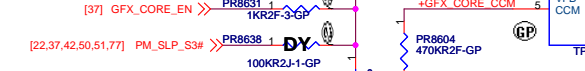
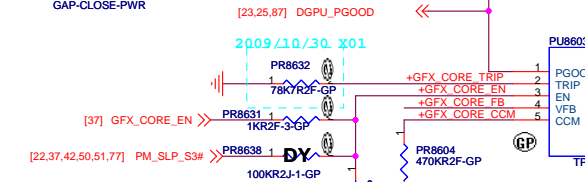
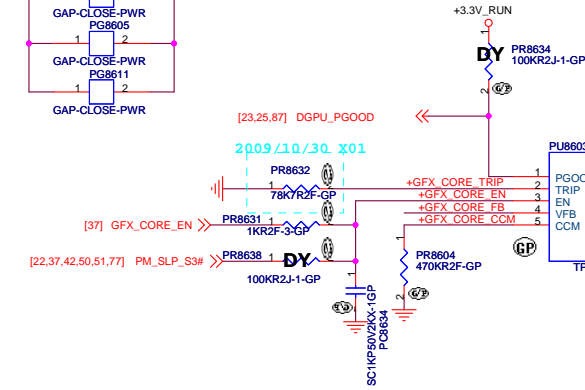
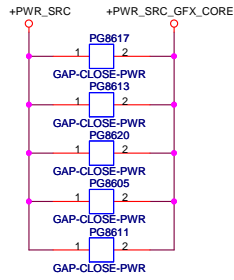
www.aitech1.ru



«Core Design»

SSID = PWR.Plane.Regulator_GFX

$$V_{out} = 0.704V * (R1 + R2) / R2$$



Frequency setting

470K -->290KHz
200K -->340KHz
100K -->380KHz
39K -->430KHz

2009/10/30 X01

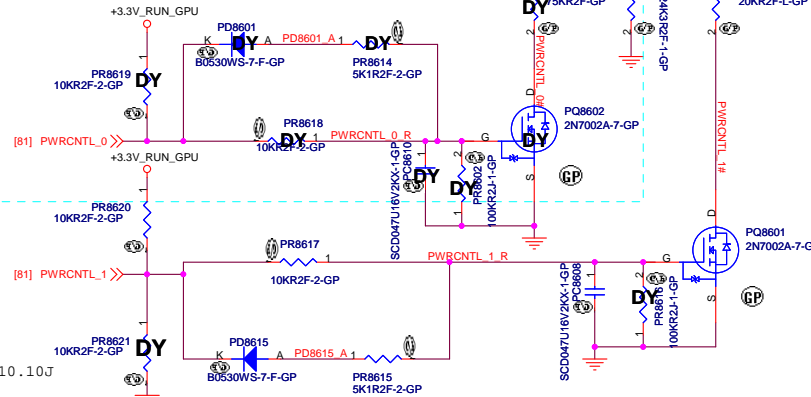
PWRCNTL_0	PWRCNTL_1	+VCC_GFX_CORE
L	H	1.03V
L	L	0.85V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMCL04T-1R5MN Cynotec DCR:4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V EEP5X0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/ 11mOhm/ 14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/ 6.1mOhm@4.5Vgs/ 84.00460.037
Switching freq-->350KHz

DW
12/07 Item 1

DIS
Thermal Design Current = 12.9A
Max Current = 16.77A
18.45A<OCP<21.81A

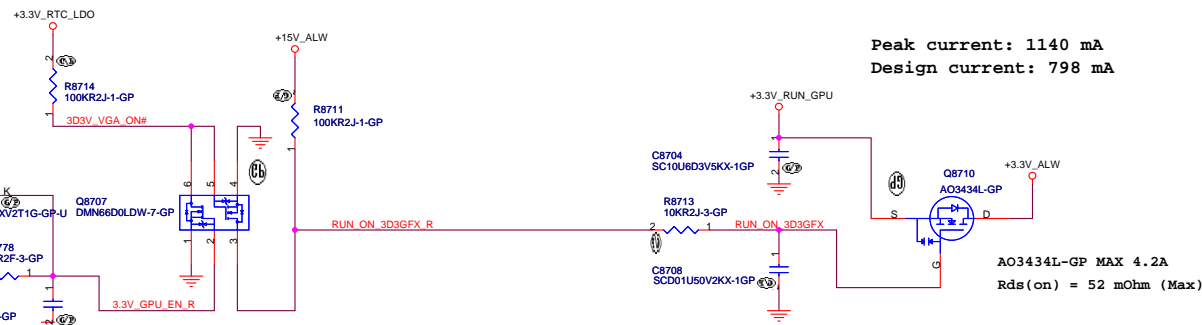
www.aitech1.ru



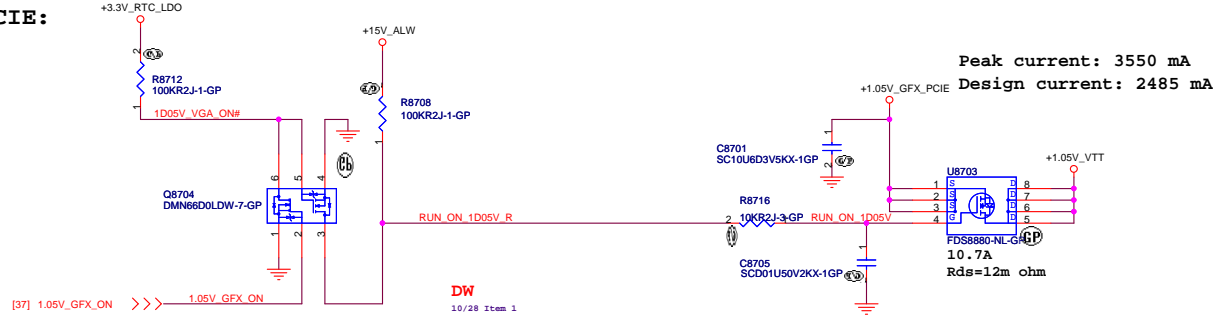
<Core Design>

DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>TPS51218 +VCC GFX CORE</i>			
Size	Document Number		Rev
Custom	<i>Vostro Calpella (Discrete)</i>		<i>X01</i>
Date:	Monday, January 18, 2010	Sheet 86 of 91	

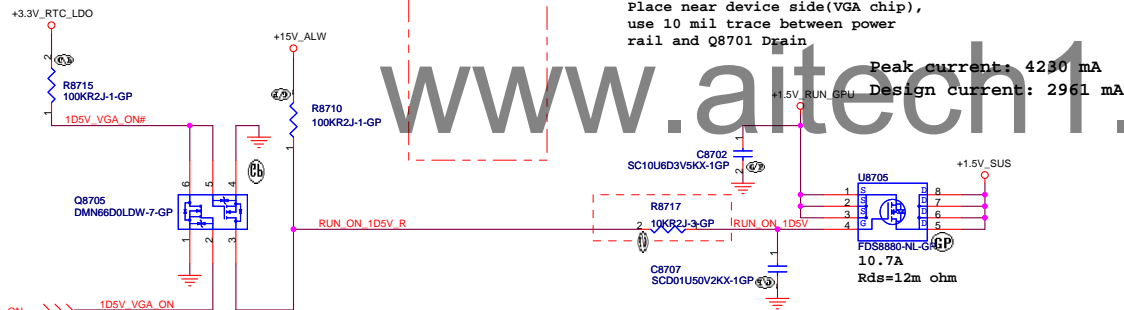
+3.3V_RUN_GPU



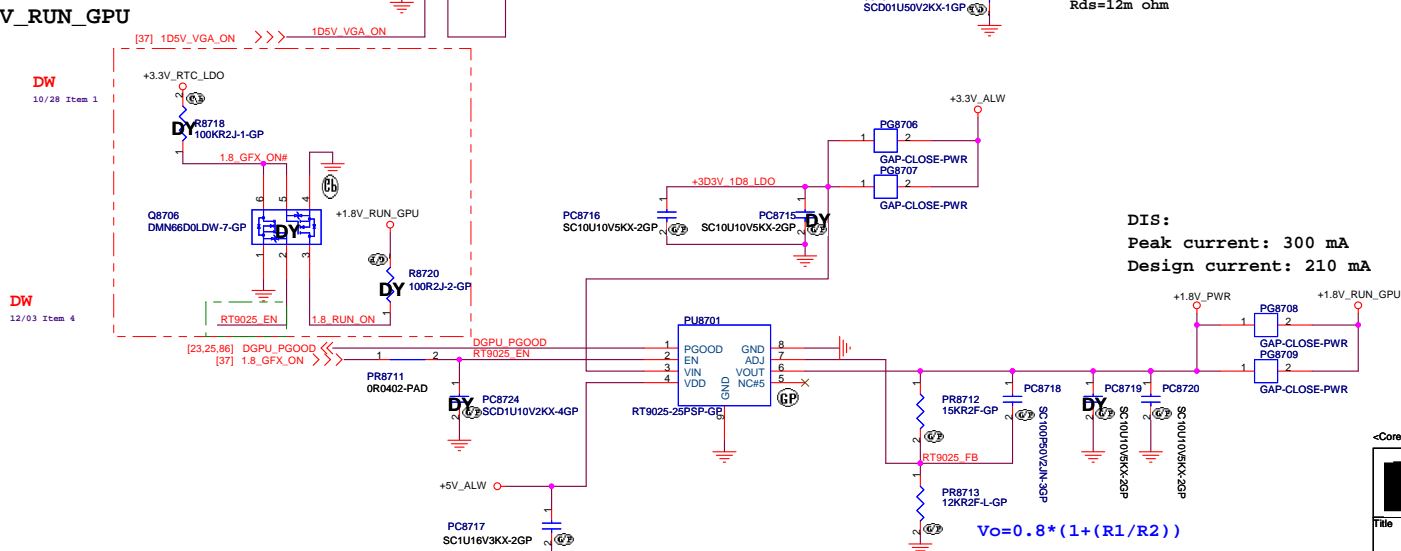
+1.05V_GFX_PCIE:



+1.5V_RUN_GPU:



+1.8V_RUN_GPU



<Core Design>

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Heichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		LDO 1.8V	
Size	Document Number	Rev	
Custom	Vostro Calpella		X01
Date:	Monday, January 18, 2010	Sheet	87 of 91

DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
2009/10/15	X01	1	25	Swapped Q2515 C,E Pin	For correct.	EE
		2	All	Combine pull-up/down resistors from single to series resistor	For save more part counts	EE
		3	37	Update 10mW circuit.	For DC mode power consumption can be less than 10mW under S5.	EE
		4	22	Add U2213,R2221	Added 3v/5v S5 power good to control resume reset sequence circuit prevent RTC data loss.	EE
		5	51	stuffed PC5105 with 1uF	For power sequencing of +1.8V_RUN , Delay timing	EE
		6	23	Added 25M Crystal	For DCI (DisplayClock_Integration)	EE
		7	79	Added BOSS4	For Steady the thermal module	EE
		9	All	BOSS1 from 34.4W005.001 to 34.4CQ03.101 CON3 from 20.K0315.005 to 20.K0293.006 CON4 from 20.K0315.028 to 20.K0275.028 CON6 from 20.K0315.036 to 20.K0276.036 DM1 from 62.10017.U81 to 62.10017.P31 DM2 from 62.10017.U71 to 62.10017.Q31 HOLE1 from ZZ.00PAD.I71 to ZZ.00PAD.G51 HOLE2 from ZZ.00PAD.K81 to ZZ.00PAD.E11 HOLE3 from ZZ.00PAD.N81 to ZZ.00PAD.D71 HOLE4 from ZZ.00PAD.N81 to ZZ.00PAD.D71 HOLE5 from ZZ.00PAD.K11 to ZZ.00PAD.E11 HOLE6 from ZZ.00PAD.I71 to ZZ.00PAD.G51 HOLE7 from ZZ.00PAD.I71 to ZZ.00PAD.G51 HOLE8 from ZZ.00PAD.N91 to ZZ.00PAD.D31 HOLE9 from ZZ.00PAD.J01 to ZZ.00PAD.D11 LCD1 from 20.F1093.040 to 20.F1555.030 TPAD1 from 20.K0320.004 to 20.K0265.004	For ME request Changed connect PN:	ME
		1	37,87	Removed CAPA_RST# from Capacity board		EE
				Added Switch Baord Detection circuit	For software request.	EE
		1	77	Reversal CON6 Pin 36 <-> 1 ; 35 <-> 2	For new connect pin define.	EE
		2	9,27	Changed RN907,L2701,L2704	For update components	EE
		3	74	Swapped the RN7408,RN7409,RN7410,RN7411	For Layout request.	EE
2009/10/16						
2009/10/19						

<Core Design>

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		Change List - EE(1)	
		Title	Rev X01
Size Custom	Document Number Vostro Calpella	Date: Monday, January 18, 2010	Sheet 88 of 91

DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
2009/10/19	X01					
		2	81	Remove R8149	For EMI team request	EMI
			21	PCLK_FWH、CLK_PCI_FB、PCLK_KBC、PCLK_TPM reserve by pass cap		
			23	CLK_PCH_48M reserve by pass cap		
			23	Romove R2350 and C2324		
2009/10/22		37	Romove R3726 and C3704			
		79	Reserve +PWR_SRC to GND cap			
	3	79	Add EC7934 0.1u in +VCC_CORE	For EMI team request	EMI	
			Add EC7911 0.1u +1.5V_SUS to GND cap*1			
			Add EC7935,EC7936 0.1u +1.5V_SUS to GND cap*2			
			Add EC7937 0.1u +1.5V_SUS to GND cap*1			
			Add EC7938 0.1u +PWR_SRC to GND cap*1			
2009/10/23			Update TR6304,TR6305 p/n to 68.00201.141			
	4	73	Move EC7302	For EMI team request	EMI	
		79	dummy 0.1u x 2 in green area 6135,195 ----EC7939,EC7940			
			dummy 0.1u cap in red area 1755,4435 -----EC7941			
			dummy 1000p in green area 5225,6950----EC7942			
			dummy 1000p in green area 3780,6180-----EC7943			
			dummy 104p and 1000p in green area 5385,7010---EC7944,EC7945			
			dummy 0.1u in green area 3400,6300--EC7946			
			dummy 0.1u in green area 1240,4035--EC7947			
		55	add damping 33ohm on R,G,B Singel---R5594,R5595,R5596			
	2009/12/08	SC	1	79	mount EC7948,EC7949,EC7934	For RF Team request
2009/12/09	SC	1	73	mount LECM2012H-900QT-GP in L7301	For EMI team request	EMI
		2	24,77	change R2405 from 10 ohm to 56 ohm and mount 120 ohm bead bead p/n:BLM15EG121SN1 L7702		
		3	73	mount 220p cap on EC7302 and EC7303		
		4	79	Add EC7950		

DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
2009/10/22	X011	1	46	PR4604,PR4605 --> 4.7ohm for RT, 0 ohm for TI	Change PU4603 from TP851125 to RT8205B	Power Team
				PR4622 --> 820k ohm for RT, DY for TI		
				PR4616 --> ASM for RT, DY for TI		
				PR4617 --> DY for RT, ASM for TI		
		53		PC5307 change to 68nF for Intel spec		
2009/10/29		2	50	Add 4.7uF at +PWR_SRC_1D5V	Improve Jitter issue	Power Team

www.aitech1.ru